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Voltage Mode Stability Control for Double Boost DC-DC Converter Using Digital PID Controller Based on FPGA

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ABSTRACT

The advanced boost DC-DC converter is used to overcome the low performance of boosting factors of traditional boost converter to get the stable and high output voltage from PV modules and other renewable sources. The application of Max-10 FPGA based PID controller development approach in double boost converter is presented to reduce system delay time and the output voltage ripples. This research is mainly focused on voltage-mode control in Continuous Conduction Mode (CCM) of the proposed converter. The proposed converter output under the PID controller is stable to manage the output voltage or to get the desired output voltage if the input voltage is changing. As the new finding result, if the two inductors' values of the proposed converter are the same, the switching frequency must be different and if the two inductors' values are different, the same switching frequency can be used for only this research. The same frequency of the two switches for two PWM modules is set 24 kHz to control the switch ON/OFF state in which the ripple voltage is about between 2.36% and 4.68%.

Key Words: *DC-DC Boost converter, FPGA, Continuous Conduction Mode, PID, PWM, Switching Frequency.*

1. INTRODUCTION

The renewable energy is an increasingly important, going to be the best green energy source in distribution systems. Harnessing of energy from renewable energy resource is efficient as the technology is advancing, and improving day by day. There are many ways to generate the renewable energy. Among them, Micro-grid units are more cost efficient than other ways. The solar energy source is DC source as a high-frequency AC source in micro-grid. The DC power supply source will obtain from a solar panel, photovoltaic array or an existing power supply network. Micro-grid unit supplied by various micro-sources and high step-up converter is needed to increase the output voltage level of the micro-source to reach the standard voltage level for the main electricity source.

The schematic diagram of solar energy system as shown in Figure 1.1 is a typical solar energy system. DC-DC converter converts electrical power provided from a source at a certain DC voltage to electrical power available at a different DC voltage. Design construction and control technique of DC-DC boost converter is emphasized in this research. In vehicle electric system, portable domestic usage, data centre and renewable energy system, DC-DC converters are most widely used for stabilizing in voltage level changing.

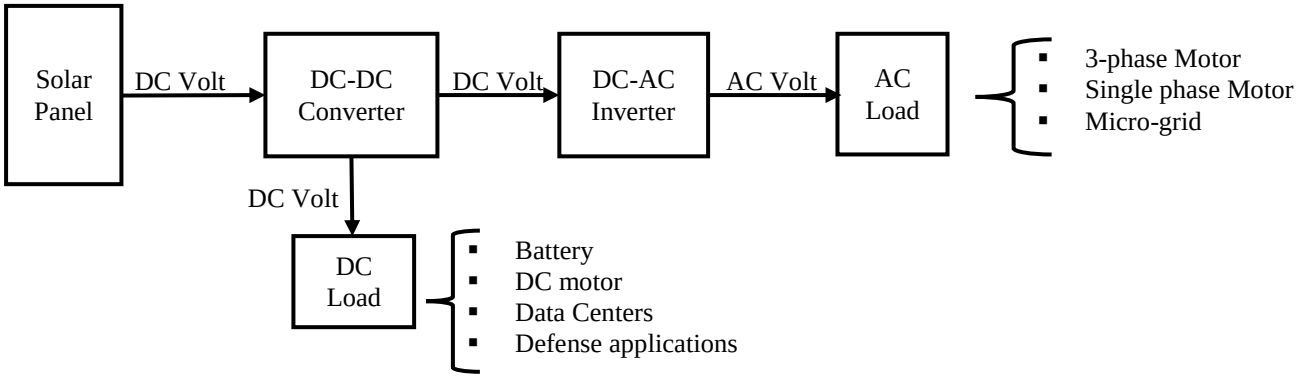

Figure 1.1: Schematic Diagram of Solar Energy System

Electrical energy, through available extensively from storage sources such as batteries, or from primary converters such as solar cells, or from distributed ac utility mains, is not easy used as such at the utilization end. DC-DC converter interfaces between the available source of electrical power and the utilization equipment with its characteristic demands of electrical power. Many a time, DC-DC converters such as Switching Mode Power Supplies (SMPS) have an unregulated input voltage. Depending on the requirements of the load, either the SMPS may step-up or step-down input voltage to produce a well regulate output load voltage. DC-DC boost converters (step-up converters) are generally applied for stabilizing a low DC voltage to a desired high voltage value. However, the traditional boost topology cannot produce a high boost state. Obtaining a high voltage is needed in some applications, which the input supply is low such as photovoltaic panel or fuel cell. The problem can be handled either by using a simple step-up converter with high duty cycle or by using cascaded converters or double boost converter.

2. RELATED WORKS

The use of a single stage in performing this conversion ratio will imply working with high duty cycles and therefore will increase the losses and reduce the voltage conversion ratio. Moreover, the use of an individual power converter with a high duty cycle to obtain high voltage conversion ratios has some design limitations due to the finite commutation times of the power devices and the size of the passive elements. If galvanic isolation is not required, the cascade connection of two boost converters can be a good alternative to obtain high voltage step-up ratios. If a large voltage or current gain is needed, it can be achieved by cascading two or more series connected boost converters. This way can give some advantages, but it creates new challenges in the same time. Circuit that is more complex, more complex controls and stability problems are main disadvantages of this approach [1]. Some previous works presented a studies of cascaded converters. Among them four previous works are discussed in this paper.

Firstly, the first work in HASSAN University, Faculty of sciences and technology of Settat, Morocco, is discussed that is using non-linear control technique in 2014. In that research, the author synthesized a robust non-linear controller of currents using a back stepping design technique with 10 kHz maximum switching frequency. A formal analysis based on Lyapunov stability and average theory was developed to describe the control currents loops performances. A classical PI controller was used for the voltage loops based on theoretically and by numerical simulations using Matlab software [2].

In second one, the authors from Department of Electrical and Computer Engineering, University of Denver, Denver, CO, USA, used a proportional-integral (PI) controller and a sliding mode controller (SMC) to control a fourth-order Boost-Boost (BB) converter in continuous conduction mode with two input switches and two output voltages in 2014. Based on the equivalent control method, a closed-loop system was developed. The resultant PI gains have a nonlinear relationship with each other. The appropriate PI gains were obtained through the least squares method. The converter under the controller is stable and robust. The maximum switching frequency was not greater than 100 KHz [3].

In third one, the authors from university HASSAN II of Casablanca, Casablanca, Morocco, also studied a double cascade boost converter based on Matlab/Simulink in 2017. The averaged fourth order nonlinear state space model in that work had described the system dynamics. Based on such a model and taking account the non-minimum phase nature of the converter, two robust non-linear controllers was synthesized using the sliding mode approach, where each controller used a different surface and a different structure. The first controller was elaborate with two nested loops. The inner currant loop was designed with the sliding mode approach and the outer voltage loop was designed with the famous PI controller. The second controller was also designed with the sliding mode approach, but this time with different sliding surface, this surface allowed to use a single control loop to regulate the currant and the voltage in the same time [4].

In last previous work, the authors from Chiba Institute of Technology, Japan, also tested the efficiency performance of cascaded double boost DC-DC converter in 2018. A setup of the cascade system with carefully selected components offered 96 % efficiency under condition with input voltage of 50 V, output voltage of 400 V and output power of 1.0 kW [5]. In controlling of

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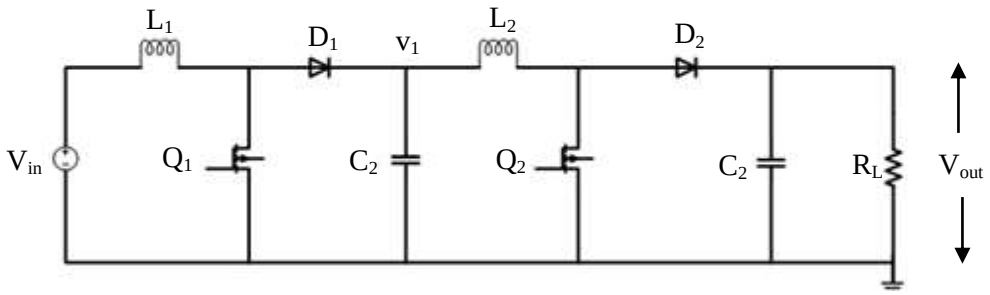
boost converter, there has mainly two types of control methods: Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM). Pulse Width Modulation (PWM) is used to generate the control pulses with constant frequency and is only be used at limited load condition. Pulse Frequency Modulation (PFM) is used to produce the control pulses at variable frequency and is especially used to regulate the output voltage at variable load conditions. Pulse Frequency Modulation (PFM) technique is implemented in a Field Programmable Gate Array (FPGA) to control DC-DC converters according to load condition. FPGA-based technique is better than the latent efficiency of the converter with processor- based technique [6].

In this paper, FPGA based voltage mode control of double boost DC-DC converter using PID controller is contributed in recent work. Moreover, the required design facts are referenced on the knowledge of revision of previous works. The logic design of ADC and PWM module are created on Max-10 FPGA. Then, the experimental test and results based on Max-10 FPGA is described in this paper.

3. DOUBLE BOOST DC-DC CONVERTER

The process of energy absorption and injection of double boost converter is performed by a combination of eight components which are two inductors, smoothing capacitor and output capacitor, two diodes and two switches. The two switches controlled the average output voltage by switching on/off duration. The converter has two distinct modes of operation: (1) continuous current conduction mode (CCM) and (2) discontinuous current conduction mode (DCM). These two modes consider the energy absorption and injection in proposed converter [2].



The most important component of this circuit is the two inductors L1 and L2 [8] and the two capacitors C1 and C2.

Equation (1) can be used to derive the inductor values.

$$L = \frac{V_{out} \cdot D(1-D)^2 \cdot T_s}{2 \cdot I_{out}(min)} \quad \text{---------- (1)}$$

Ts is the switching period. Io is the output current of the whole circuit.

Equation (2) can be used to derive the capacitor values.

$$C = \frac{D \cdot T_s \cdot V_{out}}{R_1 \cdot \Delta V_{out}} \quad \text{---------- (2)}$$

Where R is the load resistance and the ΔVo is the output ripple voltage.

The parameter values of proposed converter are presented in table 3.1.

Table 3.1. The Parameter Value

Component	Value
MIC Diode	10A10 MIC
Inductor L1 & L2	L1 = 200uH & L2 = 500uH
Switch Q1 & Q2	MOSFET IRFP450
1st Stage output capacitor (C1)	C1= 100uF
2nd Stage output capacitor (C2)	C2= 220uF
Load resistor	RL = 39 kΩ

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4. METHODOLOGY

In this work, the two stages double boost converter is analysed using pulse width modulation (PWM) control method to develop the efficiency of proposed converter. The logic design of PID controller and PWM module are created on Max-10 FPGA. Then, the experimental test and results based on Max-10 FPGA is described. The interfacing of FPGA and proposed converter is shown in Figure 4.1.

An integration between the Arduino and the FPGA allows sequential and parallel tasks to be distinguished, assigning each process to the Arduino if it the task needs to be sequential, or to the FPGA if the process can be parallelized, thus obtaining certain advantages. More than one option exists for the microcontroller/FPGA integration. In this work, physical coexistence with communication between them was chosen. They can also be integrated by means of several types of communication. Serial communication was selected as the most appropriate type due to the numbers of pins available in the FPGA. The communication would only be unidirectional, with the microcontroller sending information to the FPGA about the current angle of the robot in order for the FPGA to analyse and actuate starting from that angle. There are thus two parts in this serial communication: from the point of view of the Arduino, and from the point of view of the FPGA.

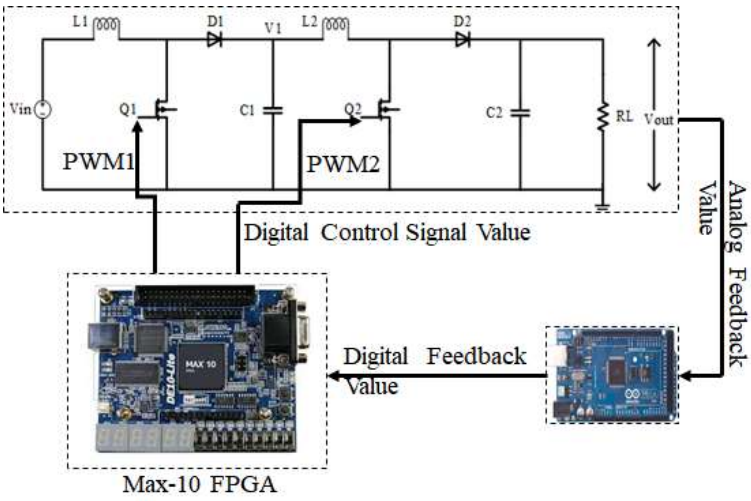

Figure 4.1: Interfacing of Proposed Converter

The application of a PID controller in a feedback control system is shown in Figure 4.2, where V_{ref} is the set point signal, V_{out} is the feedback signal, e(t) is the error signal, and u(t) is the control input to the converter.

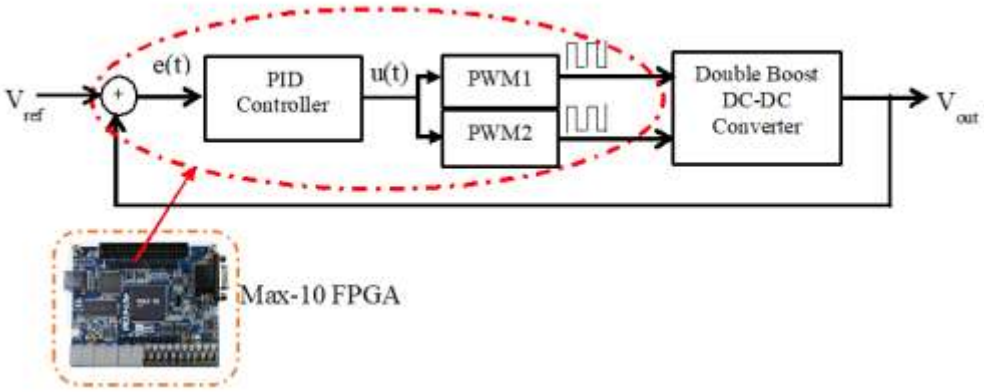

Figure 4.2: Control Design of Proposed Converter using PID Controller

The simplest form of PID controller equation is;

$$u(t) = Kp*e(t) + Ki*\int e(t)dt + Kd*de(t)/dt \text{ ---------- (3)}$$

$$e(t) = V_{ref} - V_{out} \text{ ---------- (4)}$$

The digital form of PID controller equation is

$$u(k) = u(k-1) + kp.e(k) + ki \cdot e(k-1) + kde(k-2) \text{ ----------(5)}$$

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For the realization of PID difference equation on FPGA, it must be stored all the error samples e (k), e (k − 1), e (k − 2). PID output at each clock cycle depends on present input sample e(k), previous samples e (k − 1). At each clock cycle, e(k), e (k − 1) are updated. The control signal can be saturated into a minimum (0) or maximum value (255). Since the output is restricted to 8 bits only, hence the range of output should be 0 to 255. For the implementation of decimals numbers, it has been used fixed-point arithmetic by using VHDL language.

4.1. Field Programmable Gate Array (Max-10-DE-10 Lite)

The DE10-Lite performs a reliable hardware design platform built around the Altera MAX 10 FPGA. The MAX 10 board is implemented to provide low cost, single-chip solutions in control engineering or data analysis applications and industry-leading programmable logic for ultimate design flexibility. This board comprises hardware such as USB Blaster, 3-axis accelerometer, video processing capabilities and more others. The DE 10-lite may be the perfect solution for creating, evaluating, and prototyping the desired modules of the Altera MAX 10 FPGA [7].

4.2. PWM Switching Frequency

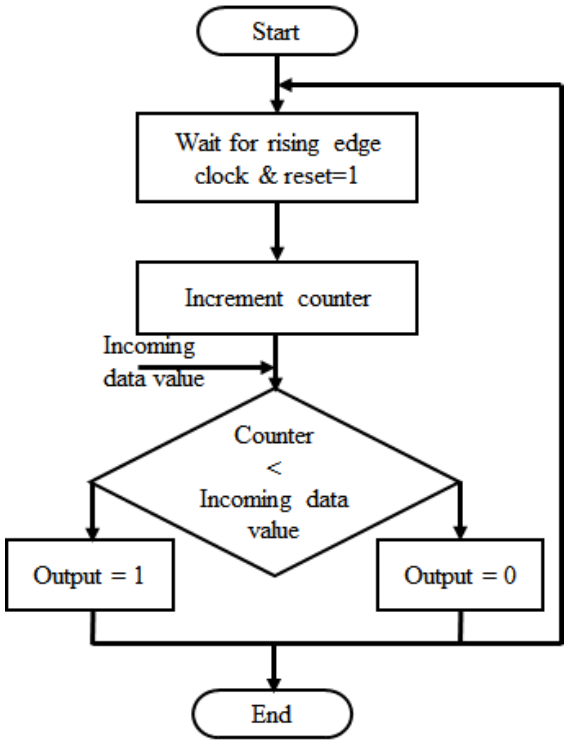

Figure 4.3: Flow chart of PWM module

The clock divider output frequency of the Max-10 FPGA is connected to the 13bit counter which counts from 0 to 8191. So, the switching frequency, 6.2 kHz is achieved. If 8kHz switching frequency is needed, the counting value will be set at 6250. The counter is a binary counter that can be set to count up or down simultaneously. Output from counter will be compared with potentiometer setting value which generates the PWM switching signal. The operation flow chart for pulse width modulation design is presented in Figure 4.3. Two PWM switching signal outputs are generated by Max-10 FPGA to feed the switching signal to two MOSFET in the proposed converter. The clock divider is applied to divide the internal clock of Max-10 board into desired frequency ranges. The desired frequency can be calculated as the following equation.

$$\text{Switching Frequency} = \frac{\text{Clock Divider Frequency}}{\text{Counter value} + 1} \quad \text{------ (6)}$$

4.3. FPGA BASED PID AND PWM MODULE

To improve the speed and minimize the cost while offering clearly good performances, the adopted architecture used includes essentially three combinational logic multipliers, one subs tractor, three adders, and eight registers. The flow chart of PID controller and PWM output is described in Figure 4.4.

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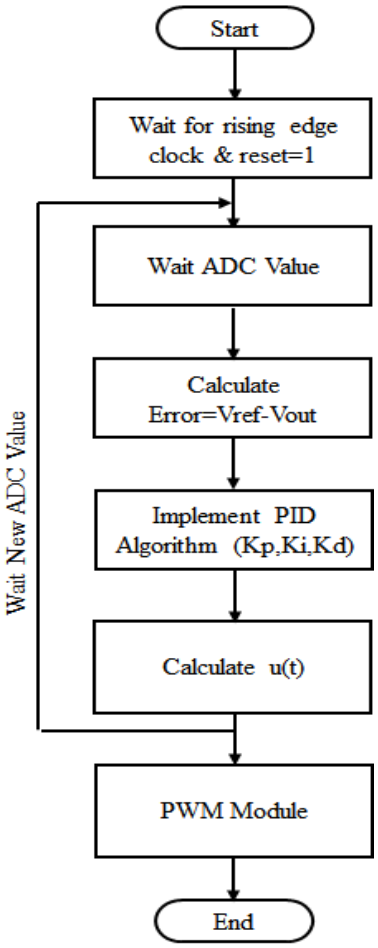

Figure 4.4: PID Controller and Two PWM Output Flow Chart

The role of FPGA, is to acquire the feedback data through ARDUINO_IO pins on FPGA. The acquired data is sent to PID controller, and then control signal is generated to two PWM modules. Building discrete PID controller on FPGA makes to increase voltage, more accurate, more power efficient and more cost effective than other digital implementation techniques. Arduino Mega 2560 is used as an Analog-to-Digital converter (ADC). It is used to send 8-bit feedback signal into the system at regular intervals of the clock. The binary value is then converted to decimal for easy operation. This decimal value is then subtracted from the set point to calculate the error value. The error is then used to evaluate the discrete PID equation and hence the control signal is generated. It is then converted back to 8-bit binary and given to two PWM modules. After that, two PWM modules generate the actual switching driven signal. Overview of input/ output parameter on max-10 FPGA device is shown in Figure 4.5. Digitally architecture of PID controller is shown in Figure 4.6. The RTL design of PID and two PWM modules are described in Figure 4.7. The Signal Tag II Logic Analyser shows the PID controller with two PWM module output as described in Figure 4.8.

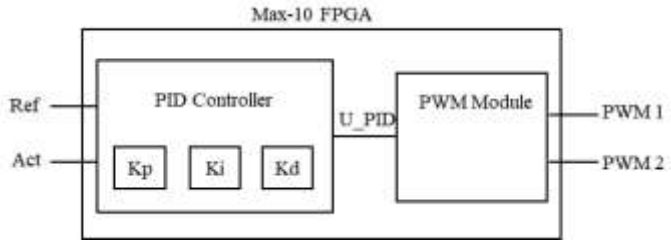

Figure 4.5: Overview of Input/ Output Parameter on Max-10 FPGA Board

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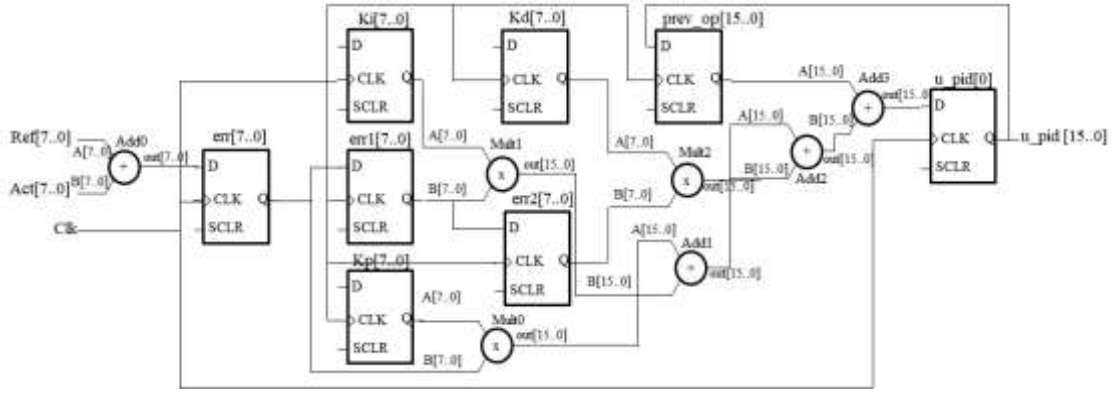

Figure 4.6: Digitally Architecture of PID Controller

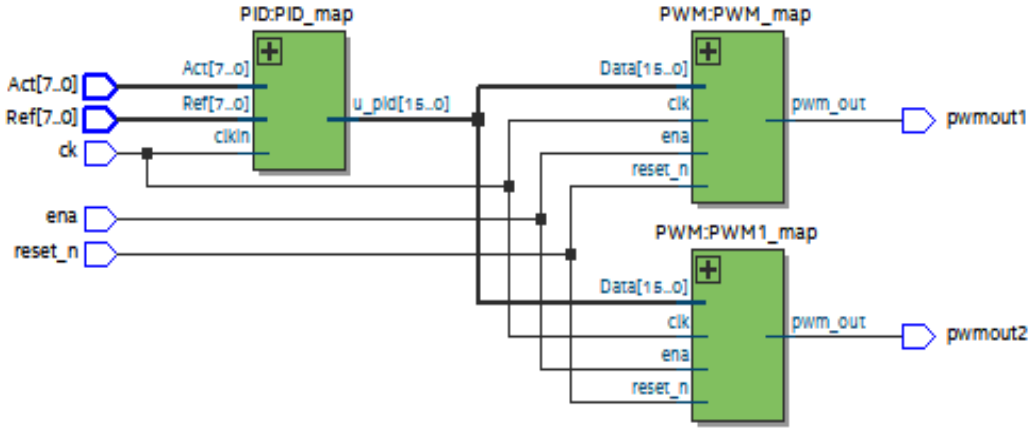

Figure 4.7: RTL Design of Two PWM Module and PID Controller Module

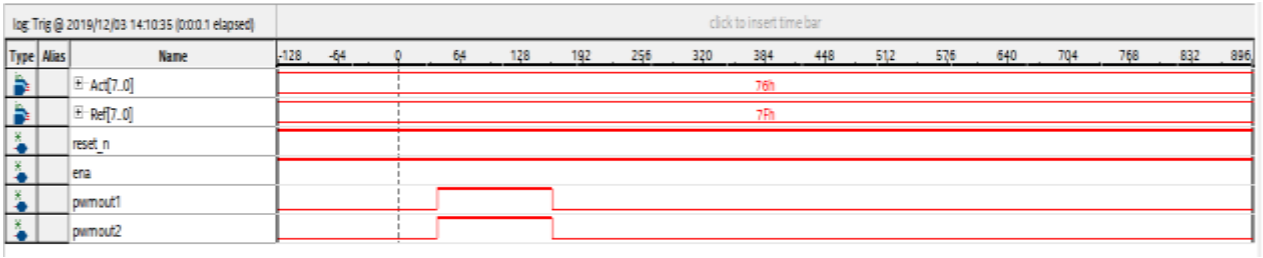

Figure 4.8: Signal Tag II Logic Analyser result of PID and Two PWM Module

To calculate error at one time, the simulation time take 0.0001us. The program execution time is 0.0008us unless sampling time consideration. The resource usage utilization and parallel compilation in FPGA are described in Table 4.1 and Table 4.2.

Table 4.1. Parallel Compilation in FPGA

	Processors	Number
1.	Number detected on machine	4
2.	Maximum allowed	2
3.	Average used	1
4.	Maximum used	2
5.	Usage by processor	%Time Used
	Processor 1	100 %

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Table 4.2 Resource Usage Summary in FPGA

	Resource	Usage
1.	Estimated Total Logic	258(1%)
2.	Total Combinational	225
3.	Logic element usage by	--
	- 4 input functions	63
	- 3 input functions	89
	- <= 2 input functions	73
4.	Logic elements by mode	
	-Normal mode	99
	-Arithmetic mode	126
5.	Total registers	89
	-Dedicated logic	89
	-I/O registers	0
6.	IO pins (Total-360pins)	21 (6%)
7.	Embedded Multiplier 9-bit	2 (<1%)

5. EXPERIMENTAL SETUP AND RESULTS OF PROPOSED SYSTEM

The experimental setup of the whole proposed system is presented in Figure 5.1. In this setup, the 12V DC power supplier is used as DC input source and digital multi-meter is used to show the output voltage from proposed converter. Two opto-couplers are used at the output side of control signal to filter some noise signals. As the manually control, Arduino Mega 2560 Board is used to implement the PID controller and to drive the ON/OFF switching time. The control switching frequency can be seen in oscilloscope display. The configuration process is generated in a bit streams design by the Quartus Prime Lite software. This design is loaded into the internal structured memory of the Max-10 FPGA.

To verify the performance of the control technique on hardware, the VHDL design code is downloaded into the target device (10M50DAF484C7G) by JTAG and the complete system is reset. The actual output data of proposed converter via Arduino Mega 2560 is read to implement PID controller as the feedback signal value. Then PID controller calculates the required control signal to drive the PWM modules. It is given back to switches of the proposed converter and once the output voltage will be produced.

The frequency of the control algorithm is 50MHz which has a period of 200µs. In order to ensure real-time operation, all separated tasks have to complete during one period of sampling frequency. All tasks are completed separately within a single sampling period. It is different for the total time of one sample processing, which can exceed duration of one sampling period. Delays that can occur as that, should be taken into account during controller design as system delays. The PWM generator has an input frequency of 50 MHz, while the generated PWM has 24 kHz, which is 2083 times smaller. This is also connected to the resolution of the PWM signal, which has resolution of a 1/2083th or 0.048% of the conduction ratio.

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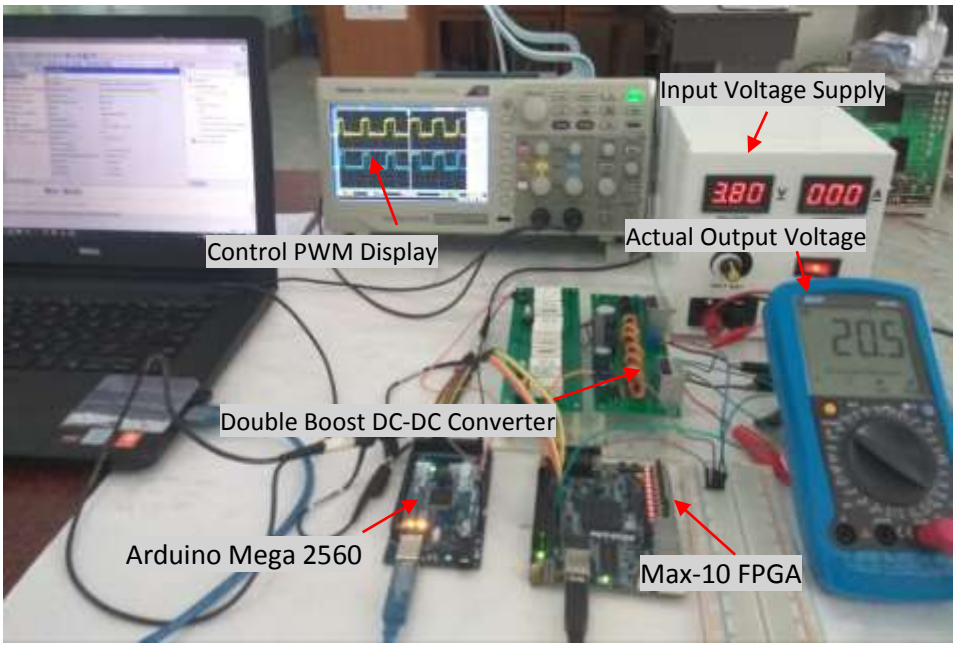
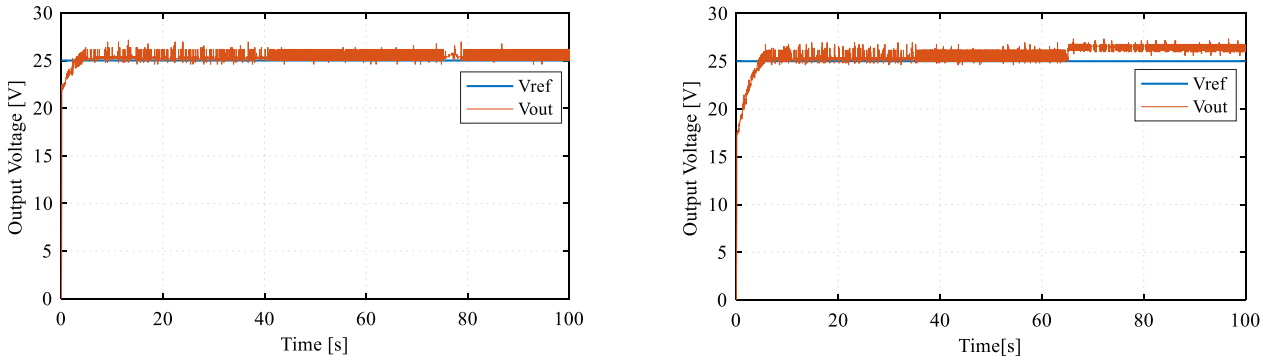


Figure 5.1: Experimental Setup of the Proposed System

When the feedback loop was implemented to open-loop control system, the system needed a controller. Thus, a PID control algorithm is designed in FPGA. The gain values of PID controller are achieved from Ziegler Nichols closed loop method Proportional gain (Kp) = 2.892, Integral gain(Ki) = 26.3 and Derivative Gain (Kd) = 0.0763 are achieved from calculation. When these parameters are implemented to controller, experimental test results of double boost DC-DC converter with variable input voltage are described in Figure 5.2.



(a) (b)

Figure 5.2: Experimental Results of Double Boost DC-DC Converter Voltage Mode Control System (a) First Testing Result (b) Second Testing Result

The input voltage range is 3V to 12V and the desired output voltage level is 25V for this experiment. The FPGA based PID controller can maintain constant output voltage very well at desired target value. The system takes nearly 2s settling time to reach the desired output voltage (25V). According to Figure 5.2, the system produces desired output voltage (25V) at Vin=5V. Experiment tested four times to confirm the best result. Each input voltage range is changed once every 20s. Once the input voltage is received, the system responds after 0.01s. Experiments show that the output tolerance of the system is at most 2V.

The maximum and minimum output voltage is measured by using data curser tool at every 60s for each test result as described in Figure 5.3. By drawing conclusions based on these results, the ripple output voltage is between 2.36 % and 4.68 % according to the difference between maximum output voltage and minimum output voltage.

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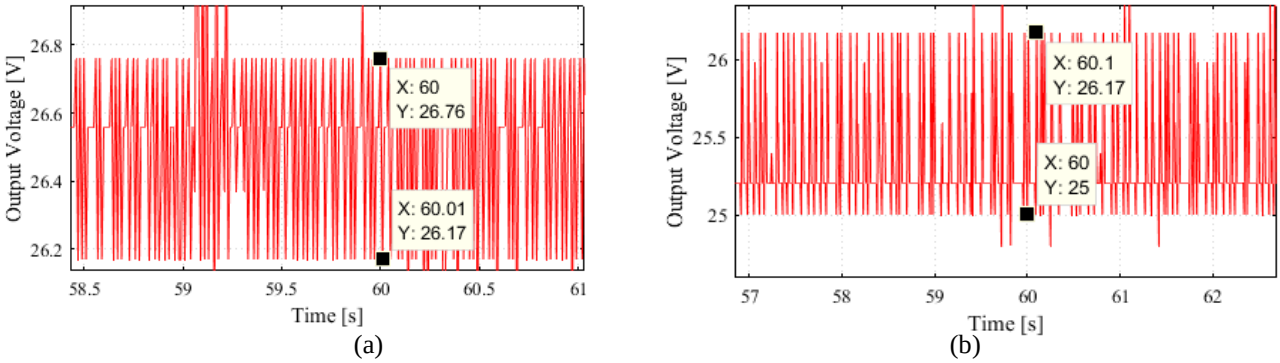

Figure 5.3 Zooming in Plot of Experimental Test Result (a) First Experimental Testing Result (b) Second Experimental Testing Result

6. DISCUSSION AND CONCLUSION

The summarizes the main points presented in this work with suggested future research on the proposed method of voltage mode control. FPGA based PWM control technique using PID is proposed, which generate the appropriate duty cycle for which the DC-DC converter can operate with and thus high output voltage can be obtained from the proposed system. The implementation of the FPGA system to control the high-performance double boost converter has been introduced. The implemented control has worked in the direction to track the output voltage by using two switches and implemented by Max-10 FPGA which is considered as an efficient hardware for rapid prototyping. XILINX FPGA Web Pack software is used to generate PWM pattern by means of VHDL program. Max-10 FPGA enables to make easy, fast, and flexible design and implementation.

In addition, a simple method of voltage controlling is used depending on the high performance of the FPGA with low resolution. Both simulation and experimental results are presented as confirmation of the approach presented. In open loop system, the system output depends on the PWM on/off time value from Max-10 FPGA in which the PWM value is command by manually using potentiometer. In closed loop system, the PID controller that is implemented in Max-10 FPGA determines PWM on/off time. In experimental results, proposed method can produce constant output voltage even the input voltage changing. The ripple voltage is 4.68%. This amount is not too much for renewable system. But it need to more good accuracy for some medical applications. As the further work, to resist the changes of load and other nonlinear disturbances, current mode control or hybrid voltage and current mode control method should be applied for this work.

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