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Design and Analysis of 2N4416 n channel JFET Single Stage Amplifier for large bandwidth and low Voltage Gain

***[1]Abdullahi Y, [2]A.A Sifawa, [3]Sulu H.T, [4]M.I Iliyasu**

[1,3,4] Department of Science Laboratory Technology,

Umaru Ali Shinkafi Polytechnic Sokoto, Nigeria

[2]Department of Physics, Sokoto State University, Sokoto, Nigeria

ABSTRACT

A bipolar junction transistor (BJT) is a current-controlled device, while a field-effect transistor (FET), is a voltage-controlled device, the bipolar transistor has two principal disadvantages. First, it has low input impedance because of the forward-biased emitter junction. Secondly, it has a considerable noise level. The field-effect transistor (FET) has a large input impedance which may be more than 100 megaohms, the FET is generally much less noisy than the ordinary or bipolar transistor. In this paper 2N4416 n channel JFET single-stage amplifier was designed, in order to analyze the circuit, important terms and main parameters were determined, the frequency response and bandwidth of the amplifier were also determined and discussed graphically using Multisim 14.2 simulator, the results characterized amplifier with large bandwidth and low voltage gain.

Keywords: Amplifier, Analysis, 2N4416, JFET n channel, Single Stage.

1.0 INTRODUCTION

The JFET stands for junction field effect transistor is a three terminal unipolar solid state device in which current is control by an electric field, there are two types of JFET, P channel and N channel JFET [1]. JFET have the following features: high input impedance, can be fabricated in small size area, it is a majority charge carrier device hence it has less noise, it is a low power consumption device, can be fabricated in small size area and occupies less space in circuits due to its smaller size [2]. Used as a switch, chopper, amplifier, buffer, in the oscillatory circuits because of its low frequency drift and in digital circuits such as computers and memory circuits because of their small size [2]. While BJT stands for bipolar junction transistor composed of p n junctions, its operation involves two kinds of charge carriers holes and electrons [3]. A BJT or FET both shares the same category of transistors, having the property of both conduction and consists of three basic terminals [3]. JFET has better thermal stability and higher input impedance than BJT; for these FETs are preferred over BJTs for use as the input stage to a multistage amplifier [4].

Many authors carried out researchers on electrical components using different simulators software packages, some of them are: Fu *et al*. [5] carried out research on Power SiC D MOSFET Model Accounting for Non-uniform Current Distribution in JFET Region, finite - element simulations show that current saturation for a typical device geometry is due to 2-D carrier distribution effects in the JFET region caused by current spreading from the channel to the JFET region. Popelka *et al*. [6] carried out research on Effect of Neutron Irradiation on High Voltage 4H-SiC Vertical JFET Characteristics: Characterization and Modeling, the 2D physical model of JFET in ATLAS simulator was developed and calibrated including the neutron irradiation effects. Simulation showed a good agreement with experimental data. Jin *et al*. [7] carried out research on Optimized Design of Space Solar Array Simulator with Novel Three-Port Linear Power Composite Transistor Based on Multiple Cascaded SiC-JFETs, Space solar array simulators (SSASs), which are used for testing space power systems generally utilize linear power topologies owing to their fast dynamic performance and satisfactory simulation accuracy. Alnasser [8] carried out research on A Novel Low Output Offset Voltage Charge Amplifier for Piezoelectric Sensors using SPICE simulator, the proposed charge amplifier was assembled by using general purpose JFET Op-Amp to capture and amplify the output voltage of the piezoelectric vibration sensor Minisense100. Narang *et al*. [9] carried out a simulation study on Impact of Temperature Variations on the Device and Circuit Performance of Tunnel FET, with ATLAS device simulation software. Taeb *et al*. [10] carried out on Modeling and analysis of a nonlinear fully distributed FET using FDTD technique , the results achieved from MATLAB are compared with semi-distributed model which is simulated by ADS simulator However some of the simulators have difficulties for beginners, in that case Proteus or Multisim can be used for their simplicity and acceptable accuracy. This paper is aimed at a design of 2N4416 JFET n channel single stage amplifier, which involves determination of the important terms, main parameters, frequency respond and bandwidth of the amplifier using Multisim 14.2 simulator.

2.0 DESIGN

2.1 The important terms to be determined

In order to analyze the 2N4416 JFET circuit, the following important terms as shown in Figure 1 are to be determined:

i. Shorted gate drain current (I_{DSS})
ii. Pinch off voltage (V_P)
iii. Gate source cut off voltage ($V_{GS\ (off)}$).

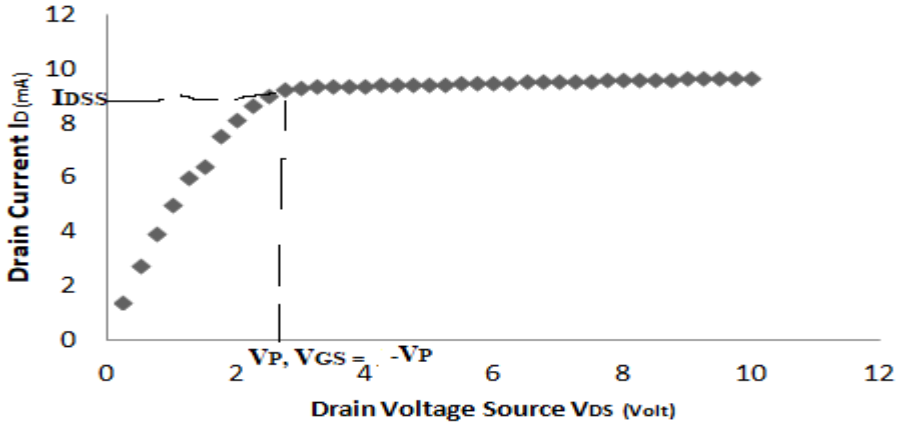

Figure 1: Relationship of Drain Current with Drain Voltage

2.1.1 Shorted-gate drain current (I_{DSS})

It is the drain current with source short circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage, it is sometimes called zero bias current. The following points may be noted carefully [11]: (i) Since I_{DSS} is measured under shorted gate conditions; it is the maximum drain current that can be getting with normal operation of 2N4416 JFET. (ii) There is a maximum drain voltage ($V_{DS\ (max)}$) that can be applied to a 2N4416 JFET, if the drain voltage exceeds $V_{DS\ (max)}$ 2N4416 JFET would breakdown (iii) The region between V_P and $V_{DS\ (max)}$ (breakdown voltage) is called constant current region or saturation region, as long as V_{DS} is kept within this range, I_D will remain constant for a constant value of V_{GS} . In other words saturation region 2N4416 JFET behaves as a constant current device, for proper working of 2N4416 JFET it must be operated in the active region.

2.1.2 Pinch off Voltage (V_P)

It is the minimum drain source voltage (V_{DS}) at which the drain current (I_{DSS}) essentially becomes constant, for values of V_{DS} greater than V_P the drain current is almost constant it is because the channel is effectively closed and does not allow further increase in drain current. It is noted that for proper function of 2N4416 JFET, it is always operated for $V_{DS} > V_P$ however V_{DS} should not exceed $V_{DS\ (max)}$ otherwise 2N4416 JFET may breakdown [11].

2.1.3 Gate source cut off voltage ($V_{GS\ (off)}$)

It is the gate source voltage ($V_{GS\ (off)}$) where the channel is completely cut off and the drain current becomes zero . Notes (i) it is interesting to note that $V_{GS\ (off)}$ will always have the same magnitude value as V_P (ii) There is a distinct difference between V_P and $V_{GS\ (off)}$. V_P is the value of V_{DS} that causes the JFET to become a constant current device, it is measured at $V_{GS} = 0$ V and will have a constant drain current = I_{DSS}, however $V_{GS\ (off)}$ is the value of V_{GS} that causes I_D to drop to nearly zero [11], [12].
Mathematical analysis yields the following expression for drain current:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \quad (1)$$

Where I_D = drain current at given V_{GS}
I_{DSS} = shorted gate drain current
V_{GS} = gate source voltage
$V_{GS(off)}$ = gate source cut off voltage .

Apart from important terms which have to be determined in order to analyze the 2N4416 JFET circuit, a 2N4416 JFET also has certain parameters which determine its performance in a circuit [12].

2.2 Parameters of a 2N4416 JFET

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In order to analyze the performance of a 2N4416 JFET in the circuit following main parameters have to be determined:

(i) a.c drain resistance (r_d)
(ii) Transconductance (g_m)
(iii) Amplification factor (μ)

2.2.1 A.C drain resistance (r_d)

It is the ratio of change in drain source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate source voltage. its unit is $\text{Volt(V)}/\text{Ampare(A)}$, expressed as [12]:

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad \text{at constant } V_{GS} \tag{2}$$

2.2.2 Transconductance (g_m)

It is the ratio of change in drain current (ΔI_D) to the change in gate source voltage (ΔV_{GS}) at constant drain source voltage (V_{DS}) it's measured in mA/volt or micromho, usually expressed as [12]:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS} \tag{3}$$

2.2.3 Amplification factor (μ)

It is the ratio of change in drain source voltage (ΔV_{DS}) to the change in gate source voltage (ΔV_{GS}) at constant drain current, expressed as:

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

The relationship among parameters can be established as under:

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiplying the numerator and denominator on R.H.S by ΔI_D we have,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \mu = r_d \times g_m \tag{4}$$

For the proper operation of n channel JFET, gate must be negative w.r.t. source [11], [12].

This can be achieved either by inserting a battery in the gate circuit or by biasing circuit. The latter method is preferred because batteries are costly and require frequent replacement.

2.3 JFET with Voltage-Divider Bias

The operating point for the circuit of d.c. conditions of JFET amplifier is V_{DS}, I_D.

But from the simulations results of 2N4416 n channel JFET at gate shorted condition ($V_{GS} = 0$) $I_D = I_{DSS} = 9.711\text{mA}$ and $V_{DS(max)} = 10\text{V}$ these are the operating point of the circuit. It is often desirable to bias a JFET near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$ for the drain voltage at midpoint ($V_D = V_{DD}/2$) [11], [12]. To produce the desired voltage drop the value R_D and R_S can be calculated using the following expression:

$$V_{DD} = I_D R_D + V_D$$

$$\therefore R_D = \frac{V_{DD} - V_D}{I_D} = \frac{(10-5)\text{V}}{4.86\text{mA}} = 1.03\text{k}\Omega \tag{5}$$

From figure7 the graph of drain current against drain source voltage we have $V_{GS\,(off)} =$ -2.75V

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$4.86 = 9.711\left[1 + \frac{V_{GS}}{2.75}\right]^2$$

$$\therefore V_{GS} = -0.8055$$

Recall, $V_G = V_{GS} + V_S$

$V_S = V_G - V_{GS}$, But $V_G = 0$, at shorted gate condition

$\therefore V_S = 0 - (-0.8055) = 0{,}8055\text{V}$, But $V_S = I_D R_S$

$$\therefore R_S = \frac{V_S}{I_D} = \frac{0.8055\text{V}}{4.86\text{mA}} = 0.17\text{k}\Omega \tag{6}$$

Also R_1 and R_2 can be calculated as follows

$$V_{DD} = I_1 R_1 + V_G$$

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$R_1 = \frac{V_{DD}-V_G}{I_1}$ but $I_1 = I_2$

$R_1 = \frac{V_{DD}-V_G}{I_2}$ and $V_2 = I_2R_2 = V_G$

$I_2 = \frac{V_G}{R_2}$

Where $V_G = V_{GS} + V_S = 0.8055 + 4.86mA \times 0.17k\Omega = 0.8262V$ and $R_2 = 1M\Omega$ usually selected

$\therefore I_2 = \frac{0.8262V}{1M\Omega} = 0.0000008262 = 0.8262\mu A$, $R_1 = \frac{10-0.8262}{0.8262\mu A} = 11k\Omega$

$\therefore R_1 = 11k\Omega$ and $R_2 = 1M\Omega$ (7)

This is the d.c. equivalent circuit which will determine the operating point (d.c. bias levels) for the circuit while in an a.c. equivalent circuit which determines the output voltage and hence voltage gain of the circuit. Here the designer intentionally selects capacitors that are large enough to appear as short circuit to the a.c signal [12]. In this case an electrolytic capacitor C_{in} ($\approx$10 µF) is used to couple the signal to the base of the transistor, a source bypass capacitor C_S ($\approx$100µF) is used in parallel with R_S to provide a low reactance path to the amplified a.c. signal and a coupling capacitor C_C ($\approx$ 10µF) couples one stage of amplification to the next stage. The complete JFET amplifier circuit with voltage divider biasing of 2N4416 n- channel common source configuration transistor is shown in Figure 2 and Figure 3.

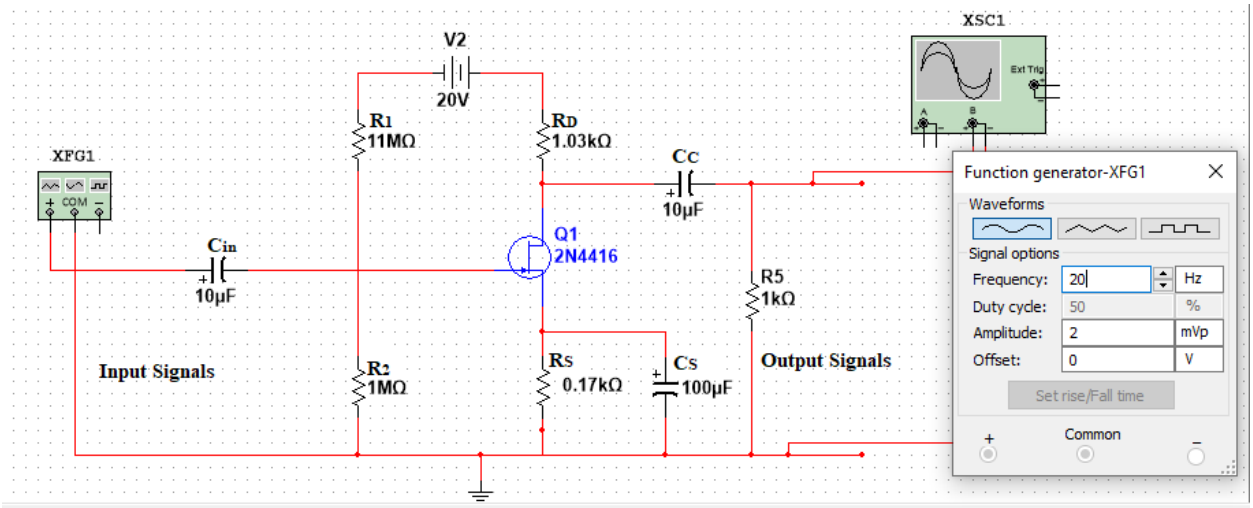

Figure 2: The complete circuit of 2N4416 n channel JFET common source configuration transistor loaded amplifier with voltage divider biasing

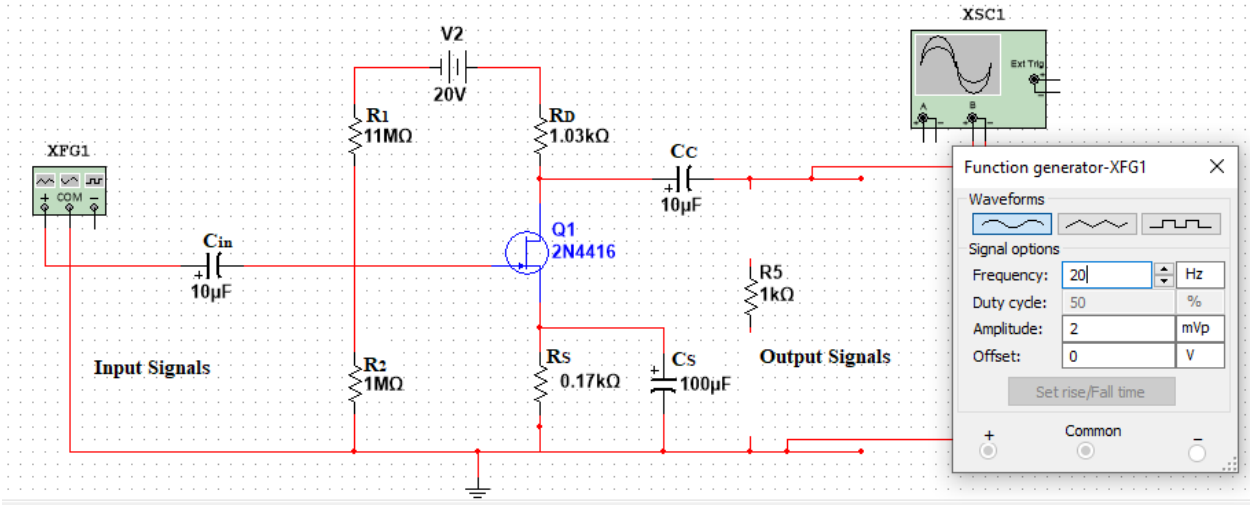

Figure 3: The complete circuit of 2N4416 n channel JFET common source configuration transistor unloaded amplifier with voltage divider biasing

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2.4 Voltage Gain of JFET Amplifier

The voltage gain of this amplifier can be calculated mathematically as follows; let $R_1 \parallel R_2$ be replaced by a single resistance R_T. Similarly, $R_D \parallel R_L$ and can be replaced by a single resistance R_{AC} (= total a.c. drain resistance) [12]. Then output voltage (V_{out}) is given by:

$V_{out} = i_d R_{AC}$

Recall, $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ or $\frac{i_d}{V_{gs}}$

$i_d = g_m V_{gs}$, But $V_{gs} = V_{in}$

$\therefore V_{out} = g_m V_{in} R_{AC}$ And $\frac{V_{out}}{V_{in}} = g_m R_{AC}$

Where $\frac{V_{out}}{V_{in}}$ = voltage gain (A_v) of the amplifier

$\therefore$ valtage gain $A_v = g_m R_{AC}$ for loaded and $g_m R_D$ for unloaded amplifier without source resistance.

With source resistance can be calculated as follows:

$V_{in} = V_{gs} + i_d R_s$

$V_{out} = i_d R_D$

Voltage gain, $A_v = \frac{V_{out}}{V_{in}} = \frac{i_d R_D}{V_{gs} + i_d R_s} = \frac{g_m V_{gs} R_D}{V_{gs} + g_m V_{gs} R_S} = \frac{g_m V_{gs} R_D}{V_{gs}(1 + g_m R_S)}$ $(i_d = g_m V_{gs})$

$\therefore A_v = \frac{g_m R_D}{1 + g_m R_S} = \frac{g_m R_D}{1 + g_m R_S}$ for unloaded and $\frac{g_m R_{AC}}{1 + g_m R_S}$ for loaded amplifier with source resistance (9)

3.0 SIMULATION

3.1 Determinations of the important terms

The following important terms were determined, shorted gate drain current (I_{DSS}), Pinch off voltage (V_P) and Gate source cut off voltage ($V_{GS\ (off)}$), the proposed simulation circuit diagram at shorted gate condition is shown in Figure 4.

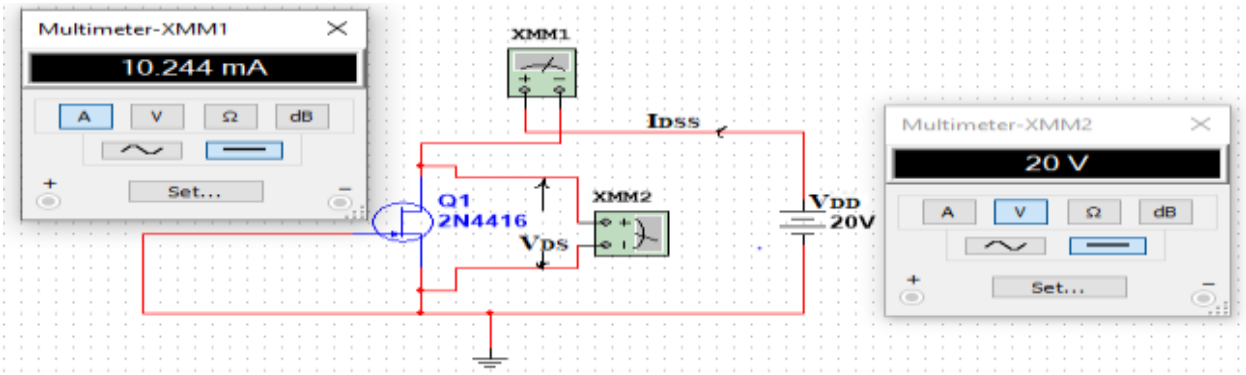

Figure 4: The simulation circuit diagram of 2N4416 n channel JFET with common source at shorted gate condition

3.2 Determinations of the main parameters

The following main parameters were determined, a.c drain resistance (r_d), transconductance (g_m) and amplification factor (μ), the proposed simulation circuit diagram is shown in Figure 5 and Figure 6.

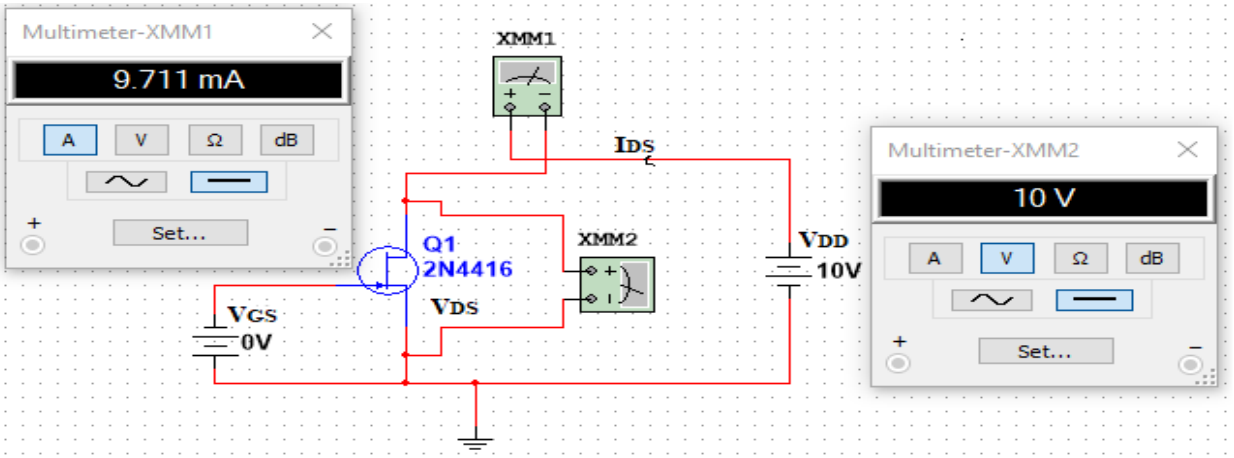

Figure 5: Shown the simulation circuit diagram of 2N4416 JFET with common source at $V_{GS} = 0$

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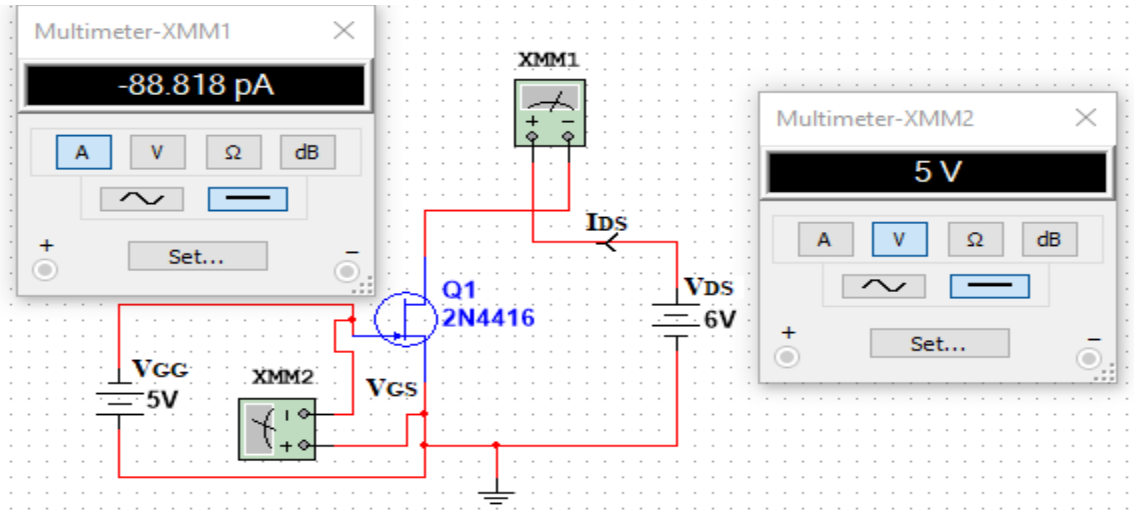

Figure 6: The simulation circuit diagram of 2N4416 JFET with common source at V_{DS} = 6V

3.3 Determination of frequency response of the amplifier

The frequency response and bandwidth of the amplifier at $V_{in} = 2mV$ and $V_{DD} = +20V$ varying the frequency of the input signal were determined; the proposed simulation circuit diagram is shown in Figure 7.

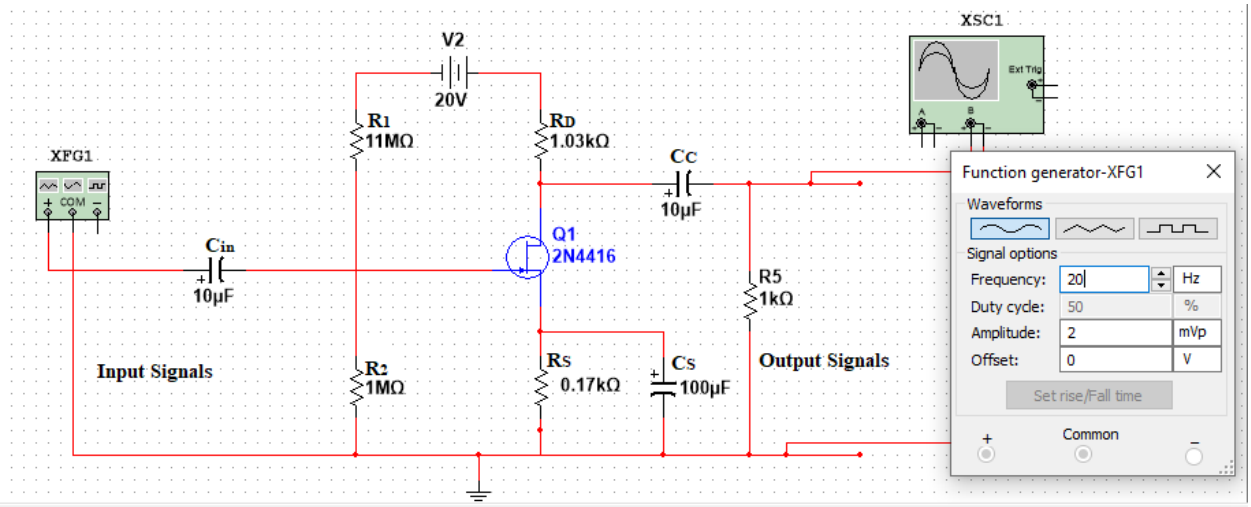

Figure 7: The simulation circuit diagram of loaded 2N4416 n channel JFET amplifier with common source at $V_{in} = 2mV$ and $V_{DD} = +20V$

4.0 RESULTS AND DISCUSSION

4.1 The important terms results and discussion

At shorted gate condition, varying the drain voltages (V_{DD}) from 0.25, 0.5, 0.75, 1 to 10V the corresponding values of drain current (I_D) and drain source voltage (V_{DS}) were obtained, the graph of I_D against V_{DS} was plotted, the shorted gate drain current (I_{DSS}), pinch off voltage (V_P) and gate source cut off voltage ($V_{GS\ (off)}$) were determined graphically as shown in Figure 8.

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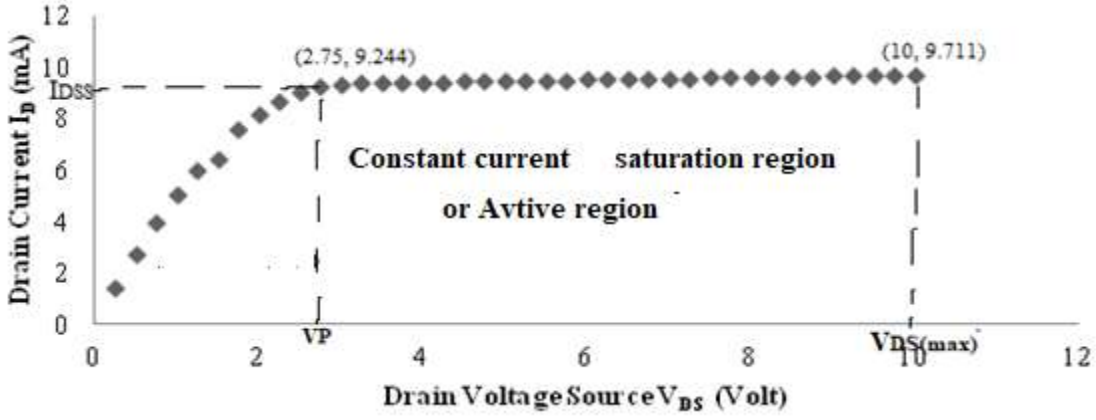

Figure 8: The graph of drain current against drain source voltage

Looking from the graph the maximum shorted gate drain current (I_{DSS}) which have been measured under shorted gate condition is 9.244mA, the minimum drain source voltage at which the drain current becomes constant is 2.75V, this is the pinch off voltage (V_P) and gate source cut off voltage ($V_{GS\ (off)}$) is -2.75V

Since the two values are always equal and opposite, the region between V_P and $V_{DS\ (max)}$ is called constant current or saturation region as long as V_{DS} is kept within this range the I_D will remain almost constant for a constant value of V_{GS}.

4.2 The main parameters results and discussion

At constant gate source voltage (V_{GS} = 0) varying the drain voltages (V_{DD}) from 1, 2, 3, 4 to 5V the corresponding values of drain current (I_D) and drain source voltage (V_{DS}) were obtained, the graph of I_D against V_{DS} was plotted and the a.c drain resistance (r_d) was determined from the graph as shown in Figure 9.

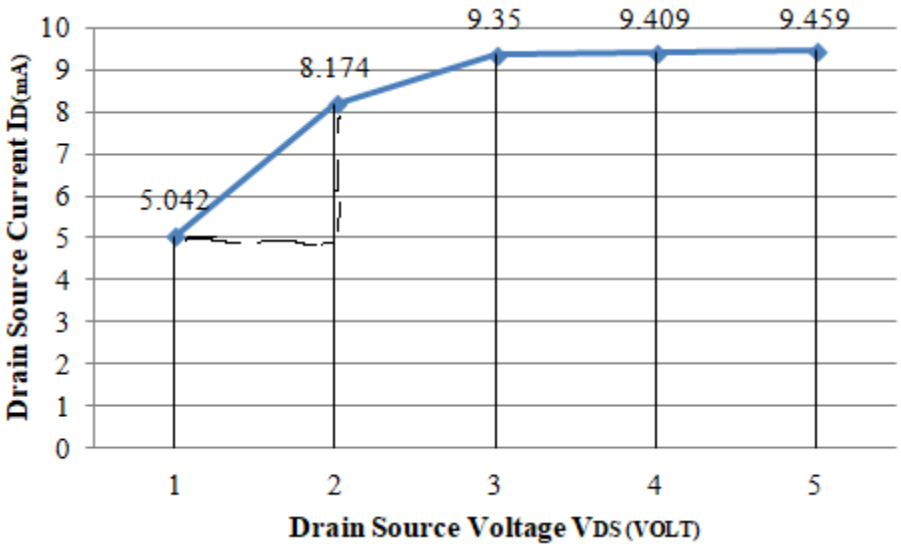

Figure 9: The graph of drain current (I_D) against drain source voltage (V_{DS}) for a.c drain resistance (r_d) determination

Looking at the first data point from the left to right of figure 8 graph the following readings were obtained:

Change in drain source voltage, $\Delta V_{DS} = 2 - 1 = 1V$

Change in drain current, $\Delta I_D = 8.174 - 5.042 = 3.132mA$

$\therefore$ a. c drain resistance $(r_d) = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1V}{3.132mA} = 0.3193k\Omega$ or 319.3Ω

Also at constant drain source voltage (V_{DS} = 6V) varying the gate voltages (V_{GG}) from 0, -1, -2, -3, -4, to -5V, the corresponding values of drain current (I_D) and drain source voltage (V_{GS}) were obtained, the graph of I_D against V_{GS} was plotted and transconductance (g_m) was determined graphically as shown in Figure 10.

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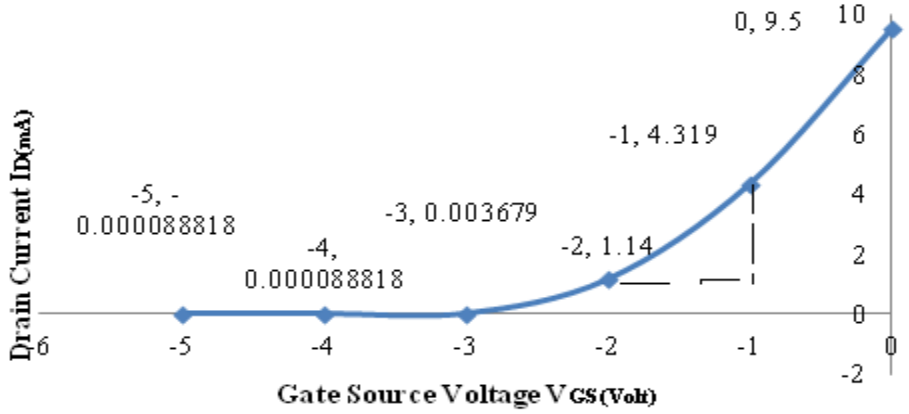

Figure 10: The graph of drain current (I_D) against gate source voltage (V_{GS}) for transconductance (g_m) determination

Looking from the graph of figure 9 the following readings were obtained:

Change in gate source voltage, $\Delta V_{GS} = 2 - 1 = 1V$

Change in drain current, $\Delta I_D = 4.319 - 1.14 = 3.179mA$

$\therefore$ transconductance$(g_m) = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{3.179mA}{1V} = 3.179\,{}^{mA}/_{V} = 3179\mu mho$ and amplification factor

$\mu = r_d \times g_m = 319.3 \times 3179 \times 10^{-6} = 1.0150547$ this shows the higher amplification factor.

4.3 The frequency response results of the amplifier and discussion

At constant applied voltages, $V_{in} = 2mV$ and $V_{DD} = +20V$ varying the frequency of the input signal the corresponding amplitude variation in output voltages at different values frequency were determined and the graph of gains against frequencies was plotted as shown in Figure 11.

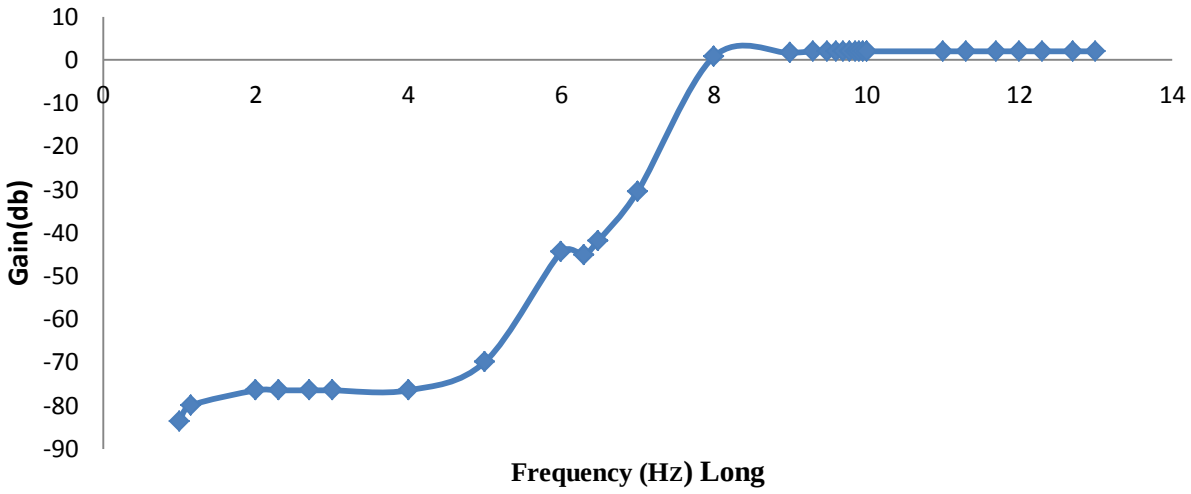

Figure11: The graph of gains against frequencies

Looking at first data point from the left to the right of the horizontal axis of figure 10 graph, the voltage gain of the amplifier increases with increases of the signal frequency, it is because reactance of the capacitors in the circuit changes with signal frequency and hence affects the output voltage and it is clear that from the frequency of log 8 which is lower cut off frequency to the infinity the gain is maximum and equal this tell the large bandwidth of the amplifier.

5. CONCLUSION

The 2N4416 n channel JFET single stage amplifier was designed in order to analyze the circuit, important terms and main parameters were determined, the frequency respond and bandwidth of the amplifier was also determined and discussed graphically, the results characterized amplifier with large bandwidth and low voltage gain, using Multisim 14.2 simulator.

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