International Journal of
Advances in Scientific Research and Engineering (ijasre)

E-ISSN : 2454-8006

DOI: 10.31695/IJASRE.2021.34102

Volume 7, Issue 11
November - 2021

Development of Counter Based Digital Capacitance Meter Implementation using Synchronized Relaxation Oscillator

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ABSTRACT

A digital capacitance meter is a piece of electronic test equipment used to measure capacitance mostly of discrete capacitors. This project presents the design and implementation of asynchronous digital capacitance meter using the principle that when a capacitor is connected across a constant DC source, it charges at an exponential rate which is dependent on the capacitance of the capacitor seen by the source as well as the resistance seen by the capacitor in the circuit. In this research, an unknown capacitor whose capacitance is to be determined was used in the timing circuit of a 555-timer base monostable (One-shot) multivibrator to give out a single pulse whose ON duration is a function of the capacitor. This pulse was synchronized to a reference clock of frequency 7.2kHz using a positive edge-triggered D flip-flop to give a count enable signal to a decade counter and ensure that the count is stopped whenever it reaches the capacitance of the capacitor used in the timing circuit. The device was tested on different capacitors (both electrolytic and ceramic) and the results of the capacitance measurement show that the device was able to measure capacitors precisely within their dynamic range of values.

Key words: *Decade Counter, Seven segments Display, Ripple counter, Clock, Flipflop, RC Timing Circuit, Astable Multivibrator, Monostable Multivibrator, Relaxation Oscillator.*

I. INTRODUCTION

In order to measure any physical quantity, that quantity should be compared with a reference value such that the ratio of the measured quantity to the reference value is a dimensionless number.

For instance, to measure the length of a book, it is compared with a graduated meter rule and the result is obtained as a dimensionless number. The same applies to a capacitance meter. A capacitance meter is a device used to measure the capacitance of a discrete capacitor[1].

Most electronic equipment's use capacitors in their circuitry which in an event of failure, suspected faulty capacitors need to be identify via troubleshooting hence a capacitance meter is used. Over the years, analog capacitance meter was the most commonly used for capacitance measurement but with the advent of allied technology and integrated circuit, digital capacitance meter has replaced the analog type because of its ease of readability, wider capacitance range, good precision measurement, cost effectiveness and portability. Fig.1 shows the block diagram of the digital capacitance meter.

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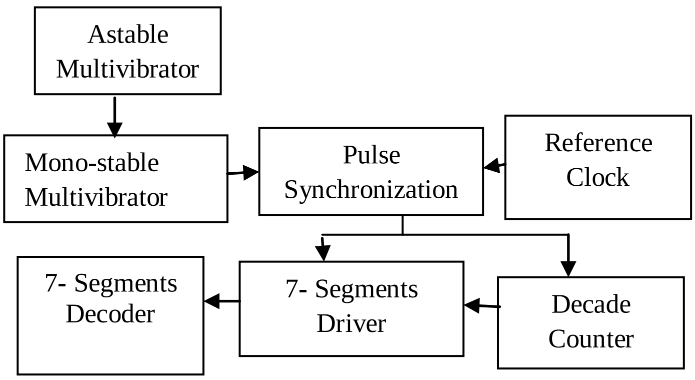

Fig 1: Digital Capacitance Meter Block Diagram

A. Block Description

1. Astable multivibrator

This was used to provide a trigger pulse to the mono-stable multivibrator so as to start its normal operation.

2. Mono-stable multivibrator

The Monostable multivibrator also called one shot multivibrator has only one resting state which is the LOW state [2]. When a trigger pulse is applied, it changes state and goes LOW for a time period which is dependent on the value of the RC timing network. This is the block where the measured capacitor is inserted. A 555-timer chip was used to implement this block.

3. Reference clock

This is where the stable clock used for counting is generated. This block also uses a 555- timer relaxation oscillator circuit to generate the required clock frequency which is fed to the counter.

4. Pulse synchronization

The mono-stable and the reference clock rising and trailing edge pulse might not coincide because of the time delay in generating them hence the need to synchronize such pulses. By synchronizing these pulses, the time delay in generating them can be removed giving a perfect alignment between the pulse edges. The pulse synchronizing circuit uses a positive edge trigger D flip-flop (7474) to provide the control pulse so as to control the counting and decoding operations.

5. Decade counter

The decade counter is used to perform the counting operation. It has an enable/strobe control terminal which is fed from the output of the pulse synchronizing circuit to initiate the counting operation as well as terminating the count whenever synchronization pulse goes LOW. CD4510 IC was used to achieved this purpose.

6. Seven segments' decoder

The decade counter provides BCD binary count which should be decoded for human interfacing hence the need for seven segments' decoder. The seven segments decoder used in this work is a BCD to decimal decoder which is fed by the counter. In this design CD4511 IC is used for this purpose and it is so selected because it has a latch for storing the count bits.

7. Seven segments display

This is where the result of the count which corresponds to the value of the capacitance will be displayed. A common cathode seven segments display was used to implement this block.

II. LITERATURE REVIEW

A capacitor also known as a charge reservoir is a device that temporarily stores charges in the electric field created between its opposite plates [3]. The increase in use of capacitors in electronic devices today cannot be over emphasized. Capacitors are used mostly in electric circuit as energy bank, when they fail the entire circuit functionality is affected hence isolating faulty capacitors in a circuit for proper functionality as well as knowing the value of an unknown discrete capacitor has attracted attention over the years which has led to emergence of research on different approaches used to measures the capacitance of a capacitor.

An Arduino based capacitance meter was designed by [4]. The capacitance measuring system is built using 3 sub-systems: Arduino board (with 12-bit internal ADC) to control the process of discharging and charging capacitor voltages using the digital Write () function, ERM20004FB-2 LCD with serial module to display measurement data and finally and RC circuit in which the measured capacitor is inserted in the C port.

A microcontroller based capacitance meter using 89C52 microcontroller for the measurement of capacitance has been design and developed by [1]. It is based on the principle of charging and discharging of the capacitor. Atmel's AT89C52 microcontroller was used. Further, an LCD module was interfaced with the microcontroller in 4-bit mode, which reduces the hardware complexity.

[5] Presents a Capacitance Meter (CM) with fast serial digital output. The CM is intended to be used as a flexible solution for interfacing multiple capacitive sensors. A special multi-slope A-to-D conversion is used, which at the end of the conversion process transforms itself into sigma/delta conversion.

DOI: 10.31695/IJASRE.2021.34102

[6] Presents an improved RC discharge capacitance meter whose principle of operation (as compared to those in Rusek and Mahmud 1986 and Hagiwara and Saegusa 1983) minimizes possible influence of the residual switch resistance and the necessity of precise adjustment of the amplifiers or buffers in the meter. The charging phase, which establishes initial conditions, is automatically monitored and the error due to limited charging time is greatly reduced without operator intervention.

III. SYSTEM DESIGN

When a capacitor is connected to a dc supply via a resistor, the capacitor begins to charge with time which is proportional to the value of the resistor and the capacitor (RC) [7], the technique employed in this research is the exponential charging and discharging of a capacitor. A reference clock (555 relaxation oscillator) is synchronized to a 555-monostable multi-vibrator (one shot relaxation oscillator) containing the unknown capacitor whose capacitance is to be determined and then fed to a decade counter which are connected in cascade arrangement. In the absence of the trigger pulse to the monostable multivibrator, the counter is RESET so that the count is zero. When the monostable multivibrator in Fig.2 is triggered by a negative going pulse, it initializes the counter to start counting the number of clock pulses passing through it until it output goes LOW at which time the counter gives a count which corresponds to the value of the capacitor.

The task at hand is to design accurately the reference clock, the monostable multivibrator with its triggering mechanism, the counter, the seven segments' drivers circuit and the display unit so that when a trigger pulse is applied, the number of clock pulses that would pass through the counter at the instant of triggering the monostable multivibrator is equal to the value of the unknown capacitor connected in the timing circuit.

A. Monostable and Clock Circuit

The mono-stable multivibrator circuit is as shown in Fig.2.

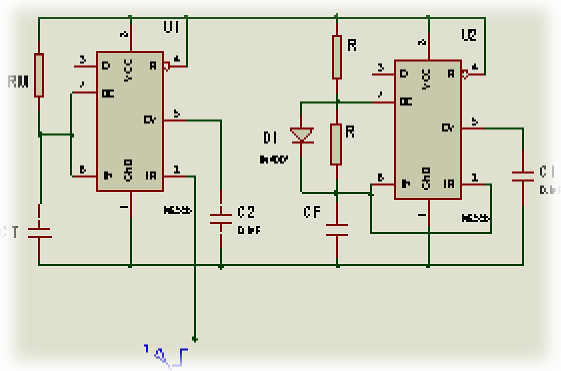

Fig 2: Monostable and Clock Circuit

Let; C_T be the capacitor to be measure,

R_T Be the charging resistor seen by C_T

For the mono-stable multivibrator, $t = 1.1C_T R_T$ and clock period $T = 1.386RC_F$

If $t = Tn$ where n is an integer and equals to count value

$1.1C_T R_T = 1.386nRC_F$ If C_T and C_F are in micro farad and that $C_F = 1\mu F$ then,

$C_T = n$ If and only if $R_M = 1.26R$ by selecting $R = 1k\Omega$ gives $R_M = 1.26k\Omega$

In practice, a $2k\Omega$ potentiometer was used for R_M instead of a fix resistor for accurate calibration of the device.

Drawback: If C_T is not an integer value, then n becomes a non-integer value which cannot be count accurately by the counter.

Solution: Since capacitors also have non-integer value, there will be no loss of generality if this capacitor value is scale by an exponent of ten and then keeping track of that scale by a decimal point. In this design a factor of 10 is used hence only one decimal point can be accommodated in the design.

How to scale: To scale C_T by a factor of ten (10), divide C_F by ten (10) so that $C_T = 0.1\mu F$

What if C_T is in nano farad?

If C_T is in Nano farad then $R_M = 1.26k \times 1000 = 1.26M\Omega$

For the same reason a $2M\Omega$ potentiometer instead of a fix resistor is selected, hence a single pole double throw (SPDT) switch can be used to connect these resistors to correspond to the value of the capacitor to be measure.

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B. Design of the Astable Multivibrator

The Astable multivibrator circuit is shown in Fig.3.

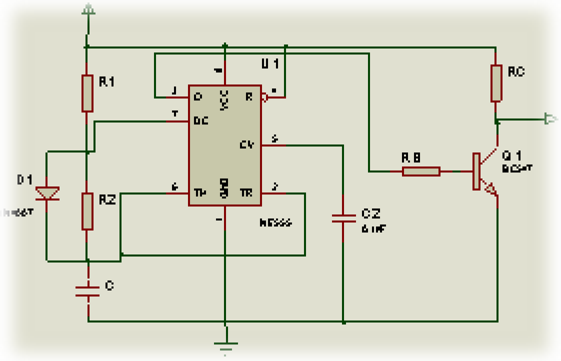

Fig 3: Astable multivibrator Circuit

The Astable multivibrator is designed to provide the trigger pulse to the monostable multivibrator.

$T_{ON} = 0.693R_1C < 1.1R_M C_T$

The worst-case design is a situation where the test capacitor is $C_T = 1\mu F$

By selecting $C = 10\mu F$ and since $R_M = 1.26k\Omega$ then,

$$R_1 < \frac{1.1 \times 1.26 \times 10^3}{0.693 \times 10} < 200$$

So, select $R_1 = 10\Omega$

Again, $T_{OFF} = 0.693R_2C >> 1.1R_M C_T$

Where the worst case designed is a situation whereby

$C_T = 1000\mu F$ Since that is the maximum capacitance value that can be read by the meter in this project.

$$R_2 > \frac{1.1 \times 1.26 \times 10^3 \times 1000}{0.693 \times 10} >> 0.2M\Omega$$

$R_2 = 10M\Omega$

For the transistor inverter designed, $\beta_{\min} = 100$

$$\frac{v_o - v_\gamma}{R_B} \times \beta_{\min} >> \frac{v_{cc}}{R_c} \text{ but } v_o = v_{cc} = 5V$$

$$\frac{5 - 0.6}{R_B} \times 100 >> \frac{5}{R_c} \qquad R_B << 88R_C$$

By selecting $R_C = 1k\Omega$ gives $R_B = 8.8k\Omega$

C. The Reference Clock Frequency

From the values obtained above it is important to compute the clock frequency

$$f = \frac{1}{0.693(1k + 1k) \times 0.1 \times 10^{-6}}$$

$f = 7.2kHz$

D. Load Modeling

From datasheet, the following information was obtained and will be used to design the circuit of Fig.4.

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Table 1: Quiescent Current of Devices

IC	Quantity	Number on chip	Quiescent -Current
CD4510	4	1	0.15mA
CD4511	4	1	0.15mA
NE555	4	1	6.00mA
7474	1	2	1.00mA

Total current drawn from the supply is obtained as;

$$4\times 0.15+4\times 0.15+4\times 6+2\times 1=27.2mA$$

$$R_L=\frac{v_o}{I}=\frac{5}{27.2\times 10^{-3}}=184\Omega$$

$$c>>\frac{1}{fR_L}=\frac{1}{50\times 184}=108.68\mu F$$

$$C=1000\mu F$$

The ripple factor is obtained as;

$$\frac{v_p}{2\sqrt{3}fCR_L}=\frac{9\sqrt{2}}{2\sqrt{3}\times 50\times 1000^{-6}\times 184}=18.8\%$$

And the diode average current is;

$$I\left(1+\pi\sqrt{fCR_L}\right)=27.2\times 10^{-3}\times(1+\pi\sqrt{50\times 1000\times 10^{-6}\times 184})$$
$$=0.286A$$

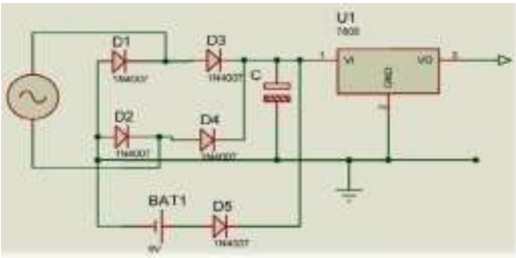

Fig 4: Power Supply Circuit Diagram

The complete circuit diagram of the digital capacitance meter implementation in proteus8.9 is as shown in Fig.5.

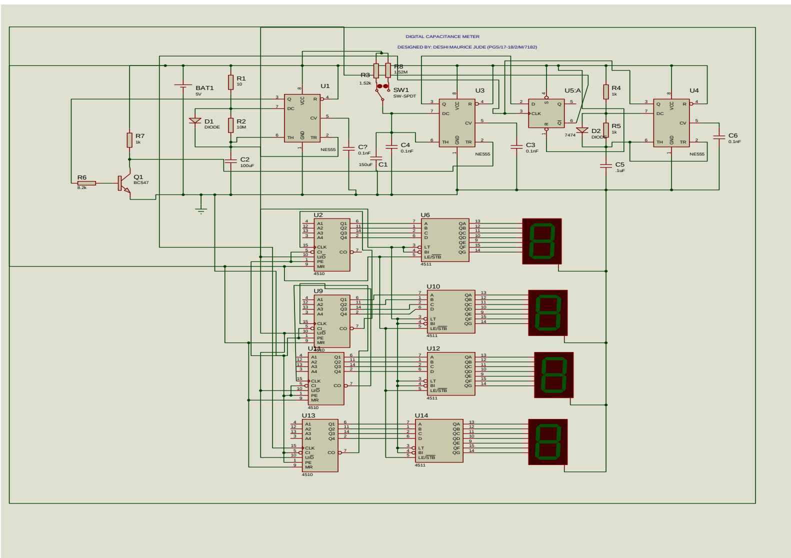

Fig 5: Digital Capacitance Complete Circuit Diagram

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IV. RESULTS OF SYSTEM TESTING

The following shows the results obtained after the system was subjected to series of test.
The output of the mono-stable multivibrator when it receives a trigger pulse and the reference clock signal are as shown in Fig.6. These pulses are synchronized via a positive edge triggered D flip-flop to control the counting operation of the decade counter.

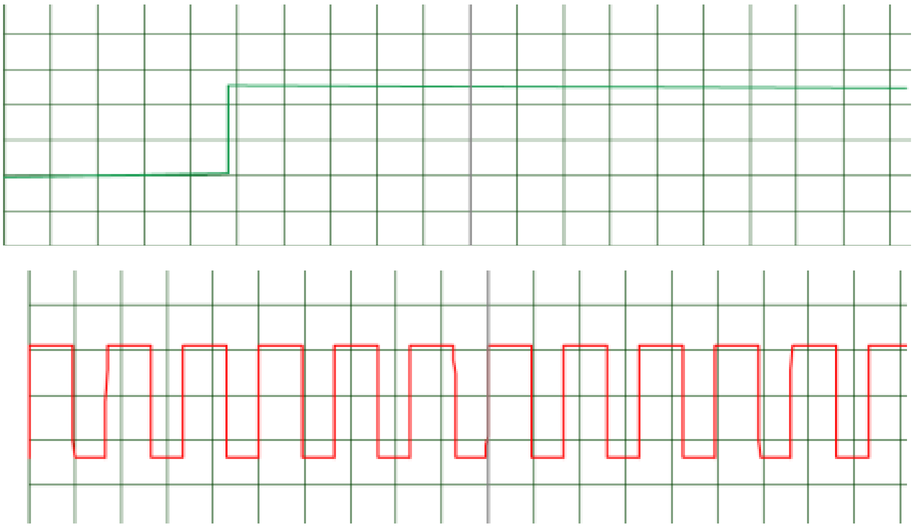

Fig 6: Monostable Multivibrator Output synchronize to the reference clock

Different capacitors were connected to the meter to measure their capacitances and the results obtained were shown in Table 2 and Table 3 for electrolytic and ceramic capacitors respectively.

Table 2: Results for Electrolytic Capacitor

Capacitance Value (μF)	Simulation Measurement (μF)	Practical Measurement (μF)
4.7	4.7	4.6
10	10	9.4
47	47	48.1
68	68	65.1
100	100	100.6
220	220	220.1
270	270	274.0
330	330	325.0
470	470	474.3
1000	1000	998.9

Table 3: Results for Ceramics Capacitor

Capacitance Value (nF)	Simulation Measurement (nF)	Practical Measurement (nF)
68	68	68.0
100	100	96.0
220	220	218.0
220	220	223.1

DOI: 10.31695/IJASRE.2021.34102

The constructed prototype model of the digital capacitance meter are shown in Fig.7 and Fig.8

Fig 7: The Digital Capacitance Meter Device

Fig 8: Digital Capacitance Meter Implementation

V. SUMMARY

This work is aimed at designing and implementing a system that can accurately measure the capacitance of an unknown capacitor. The technique adopted was the exponential charging and discharging of a capacitor when connected to a constant DC supply.

The circuit consists of three parts: control parts, counting and decoding part and the display part. The control part uses 555-timer relaxation oscillators to generate control signals to control the counting and decoding operations, while the counting and decoding part feature a ripple connected four decades counter in cascade each connected to a decoder and finally the display part uses a cascade arrangement of four seven segments' display each connected to a seven segments driver via a current limiting resistor to display the result.

Several capacitors were subjected to test and results obtained were in the acceptable range of the capacitors tolerances both for ceramic and electrolytic capacitors.

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DOI: 10.31695/IJASRE.2021.34102

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DOI: 10.31695/IJASRE.2021.34102