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Study of Impact of HfO_2 gate oxide on the Electrical Characteristics of Nanowire Junction less Transistor

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ABSTRACT

This paper proposes hafnium (IV) oxide (HfO_2) as gate oxide material of the nanowire junctionless transistor (NJT) to replace the conventional silicon dioxide (SiO_2). Leakage current usually increased due to an increase of tunneling of electrons in SiO_2 transistor when the thickness oxide (t_{ox}) of the gate material is below 2nm. The main advantages of HfO_2 is high dielectric constant k of 20 to 25 which is almost 6 times than that of SiO_2. Similarly, HfO_2 has an energy band gap of 5.3 to 5.7eV. As a result, low leakage current and short channel effects (SCEs) was experienced. An increased in the gate capacitance of the device leads to improve the performance of the device without affecting the enhanced leakage current. All these was achieved by designing and simulating the device using the SDE tools of Sentaurus TCAD. Electrical characteristics was extracted using the Sdevice tools of the software. The performance was significantly increased to approximately 10^{10} using HfO_2 material.

Key Words: Dielectric constant, Gate oxide, Hafnium dioxide, Junction less Transistor, leakage current.

1. INTRODUCTION

As the scaling of conventional planar transistor device reached its limit, leakage current and short channel effects (SCEs) increases. Subthreshold slope (SS) and drain induced barrier lowering (DIBL) are the main examples of SCEs [1]. The restriction enforced on electron drift characteristics in the channel, threshold voltage variation, reduction in performance ratio of the device and increases of leakage current causing the scaling of conventional CMOS transistors of gate length less than 10nm technologies nearly difficult. Reduction of the performance, I_{ON}/I_{OFF} ratio of the transistors, causes unsteadiness of transistor device and limits subthreshold circuit design. Similarly, when a leakage current increased, the static power consumption also increased [2, 3].

Movement of electrons in the NJT channel is controlled by gate oxide. Electrical characteristics of the gate oxide are critical to the realization of the conductive channel region of the device below the gate [4]. conventional gate oxide material used in NJT is SiO_2 which has been used in many researches. As the scaling of NJT device increases, t_{ox} steadily reduces in order to increase gate capacitance, hence increases the device performance [5]. Leakage currents drastically increased due to tunnelling of electrons when the tox is below 2nm. High leakage current leads to poor reliability and high power consumption of the device [6]. High k dielectrics such as hafnium oxide (HfO_2) is a good alternative to replace the conventional SiO_2 thereby increasing the gate capacitance without affecting the leakage [7].

In this research, two NJTs of different gate length and constant nanowire diameter (DNW) of 4nm was designed and simulate using SDE tools of sentaurus TCAD. Two different gate oxides, HfO_2 and SiO_2 gate oxides of tox 1nm was used in each device. I-V characteristics was extracted using the Sdevice Tools of the sentaurus. Electrical characteristics such as leakage current, drain induced barrier lowering (DIBL), subthreshold slope (SS), On-state current, performance ratio etc. were compared and analyzed.

2. RESEARCH OBJECTIVE

The aim of this research is to study the impact of HfO_2 agate oxide on the electrical characteristics of junctionless nanowire transistor of different gate lengths and constant nanowire diameter of 4nm.

The objectives of this study are:

i. To design and simulate a nanowire junctionless transistors with HfO_2 and SiO_2 gate oxides.

ii. To extract the electrical characteristics such as DIBL, SS, I_{ON}, I_{OFF} etc. of the two devices.

iii. To compare and analyze the electrical characteristics of the two devices in order to get the most optimized device

3. PREVIOUS WORK

High k dielectrics materials have good chemical and thermal stability on silicon material [8]. Reduction of the oxide thickness of the NJT gate to 1nm leads to high leakage current in SiO_2 device. HfO_2 have higher dielectric constant (k) is necessary to reduce the leakage current. Tunneling path and the energy gap between the conduction band and fermi level of the junctionless device with HfO_2 are larger in the subthreshold state compared to SiO_2 device in the drain region. High k increases the capacitance of the device with HfO_2 thereby increasing the charge holding capacity due to large capacitance of the device [9].

Different Junctionless nanowire transistors were implemented using HfO_2 and SiO_2 gate dielectrics with tox of 8 nm and 13 nm respectively. The complex impedance plane using z-view software was found to be 2.15×10^7 Ω for HfO_2 and 3.6×10^5 for SiO_2 thin films. Higher electric resistance of HfO_2 thin films and its smaller crystallite size caused very low leakage current than SiO_2 gate dielectrics. HfO_2 shows to be a worthy dielectric in terms of Of-state current and gives suitable switching of the device. Consequently, improving the device I_{ON}/I_{OFF} ratio [10].

Two junctionless double gate MOSFET devices with SiO_2 and HfO_2 gate oxide of 22nm technology were compared and analysed. The result shows that HfO2 gate oxide device have better I_{ON}/I_{OFF} ratio, improved DIBL and SS parameters due to the fact that Junctionless double gate MOSFET has electrostatic far better than the conventional single gate device. Secondly, due to the absent of stringent requirement of high concentration gradient makes the scaling of gate oxide layers possible to around 1nm. High leakage current was observed in the device with SiO_2 gate oxide for gate thickness oxide of 1nm. Due to the high dielectric constant (k) of HfO2 a highly improved leakage current was observed [11].

High k gate stack gate-all-around silicon NJT was used for neutral biomolecule species detection and also to boost the performance of the transistor. High metal gate work function and induced gate stack. The result shows significant improved in DIBL, leakage current, SS, trans-conductance and threshold voltage when they were all examined for the study of the biosensor response. HfO_2 was recognized a better metal oxide semiconductor transistor gate oxide to diminish the gate tunneling current and short channel effects due to its thermal stability and chemical compatibility [12].

Nanoscale junctionless FinFET of different channel cross section shapes and defined thickness of back and gate oxide layers was designed and simulate. Thermal conductivity of the oxide materials and the surface contact area between the channel and the oxide layers are the main factors that define the temperature at the center of the channel. Transistor having SiO_2 as the back oxide layer and HfO_2 as the gate oxide layer, the temperature in the channel center is mainly defined by the width of the channel base in contact with the back oxide layer [13]. Gate control was increased in double hetero gate oxide device with high k dielectric such as HfO_2 on the top oxide. Due to the compatibility of lattice constant of SiO_2 and silicon, low-k dielectric can be used over silicon body. The leakage current was significantly decreased when the permittivity coefficient as well as the t_{ox} of the transistor decreased [14].

4. RESEARCH METHODOLOGY

In this work, cylindrical NJT of gate lengths of 10nm, 20nm and 50nm were designed and simulated. SiO_2 and HfO_2 were used as gate oxides. D_{NW} was constant, 4nm for all the devices. Doping concentration of $1.0 \times 10^{-19} cm^{-3}$ was used throughout the research. Thickness oxide of the two gate oxides is the same, 1nm. Gate and drain voltage of 1V as well as metal gate work function (ϕm) of 4.8 eV were used in this work. Design and simulation of the devices was done using the SDE tools of Technology Computer-Aided Design (TCAD) software, Sentaurus. Sdevice tools of the software was used to extract the electrical characteristics such leakage current, I_{ON} current, DIBL, threshold voltage, subthreshold swing and On-State to Off-state current ratio.

Philips unified mobility model and Lombardi mobility model were considered as field- and doping-dependent mobility degradation. For Dominant generation and recombination process in silicon and other indirect energy band gap materials,

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Shockley–Read–Hall was used. Also, the SRH dominate in direct band gap materials under conditions of very low carrier densities or very low level injection. Auger recombination model and Fermi–Dirac statistics were also used as design model.

Electrical parameters of nanowire junctionless transistor with HfO_2 gate oxide was compared with that of SiO_2 gate oxide device to determine the best optimized device.

5. RESULTS AND DISCUSSION

Scaling of NJT is necessary so as to have large number of transistors in a microprocessor. This could lead to improve the speed of the device. As the tox reduced to 1nm, the IOFF increases in SiO_2 device. Figure 1 shows that the leakage current of 3.3 x 10^{-13}A was experienced in SiO_2 device with gate length of 10nm and D_{NW} of 4nm. The leakage current was significantly reduced to 7.12 x 10^{-16}A in HfO^2 device having the same gate length and nanowire diameter due to its high dielectric constant and high gate capacitance. Similarly, as the gate length of the device increased, the leakage current decreased in all the transistors. For the 50nm gate length, the leakage current was 2.13 x 10^{-17}A and 3.25 x 10^{-16}A for HfO_2 and SiO_2 device respectively.

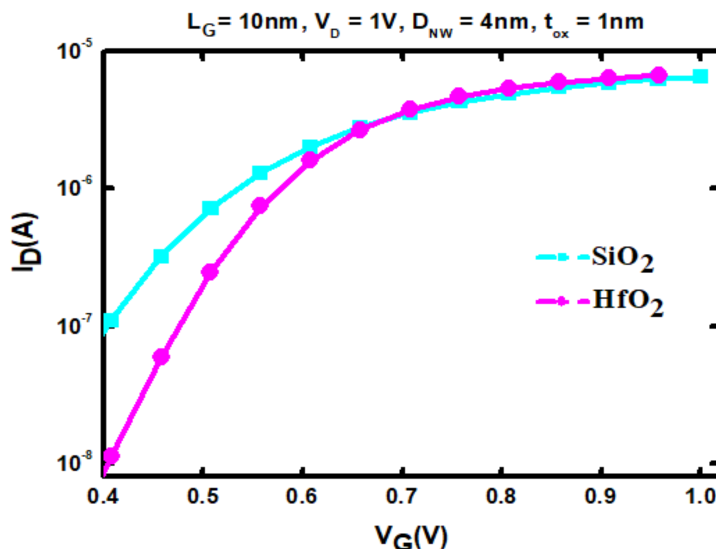

Figure 1 I-V characteristics of a Junctionless Nanowire FET

Junctionless transistor was introduced to eliminate the difficulties in scaling of transistor paramters, complex thermal budget as well as to reduce the SCEs such as DIBL and SS. It was found that the DIBL for HfO_2 device was considerably improved for gate length of 10nm to 14.74mV/V compared to SiO_2 device which have 49.16mV/V using the same gate length as shown in figure 2.

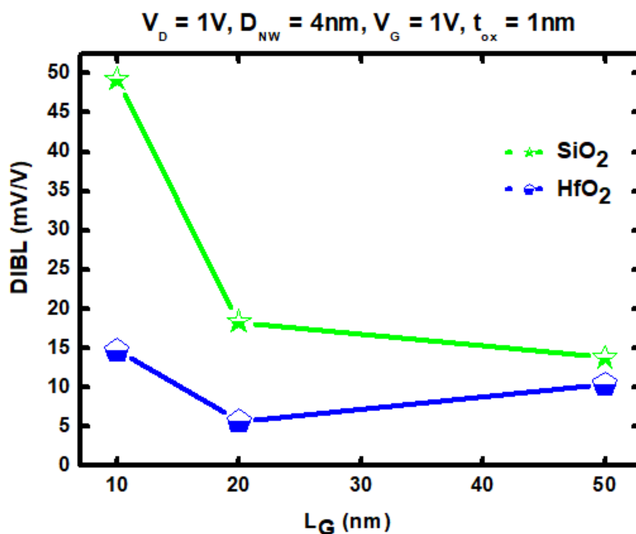

Figure 2 DIBL of different gate lengths of NJT

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Similarly, the Subthreshold slope, SS of HfO_2 device with gate length 20nm was successfully reduced to 56.34mV/dec compared to 60.85mV/dec for SiO_2 device having the same gate length of 20nm as shown in figure 3.

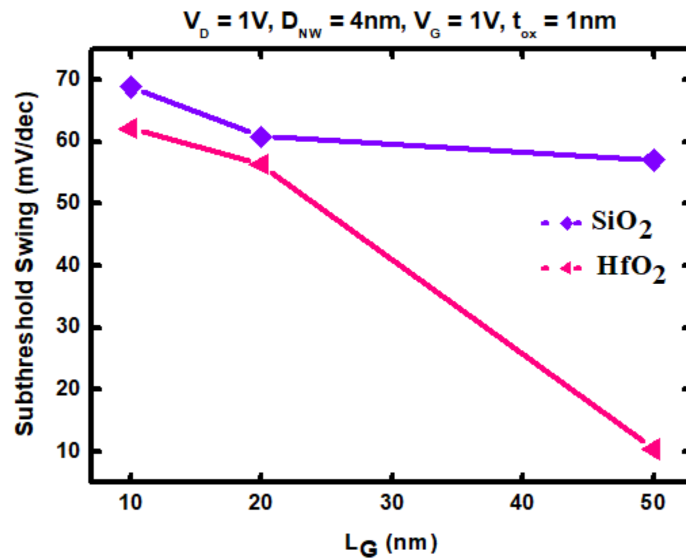

Figure 3 Subthreshold Swing of the two devices

Due to the high N_D of 1 x $10^{-19}cm^{-3}$ and small D_{NW} of the cylindrical nanowire, the On-state current (I_{ON}) of the device increased. Figure 4 shows the I_{ON} of transistor with HfO_2 gate oxide was 6.65 x 10^{-6}A while I_{ON} for SiO_2 device was 6.48 x 10^{-6}A for gate length of 10nm and nanowire diameter of 4nm. It was observed that as the gate length of all the two devices increased, the on-state current decreases. However, when the gate length was increased to 50nm, the I_{ON} was 5.996 x 10^{-6}A and 5.220 x 10^{-6}A for HfO_2 device and SiO_2 device respectively.

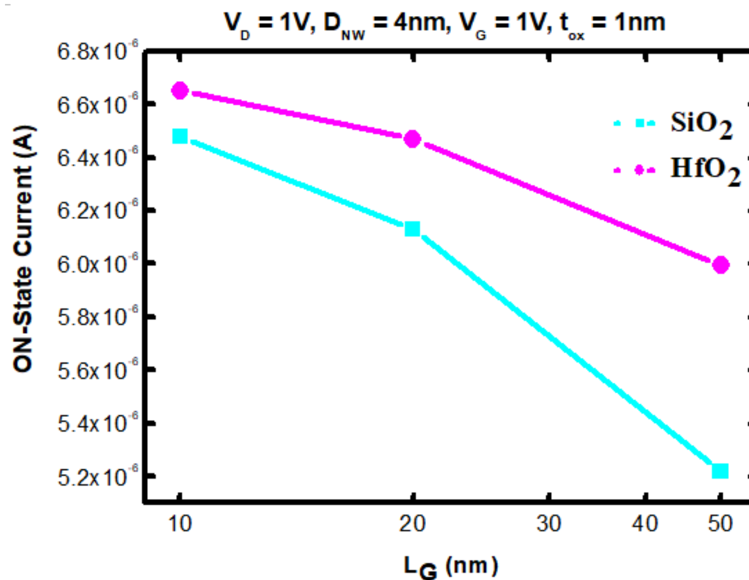

Figure 4 I_{ON} of the two devices with constant D_{NW} of 4nm and different L_G

The surface electrostatic potential in the channel region near source region is marginally increased when HfO_2 was used as gate oxide in the NJT. Therefore, the performance of the transistor was improved due to a large movement of carriers from source to channel of the device. In figure 5, I_{ON}/I_{OFF} current ratio of 9.34 x 10^9A was experienced in transistor with HfO_2 which is far better than that of SiO_2 device of 1.96 x 10^7A for gate length of 10nm and nanowire diameter of 4nm in all the two devices. This shows than the performance of junctionless transistor was highly improved when HfO_2 was used as gate oxide material.

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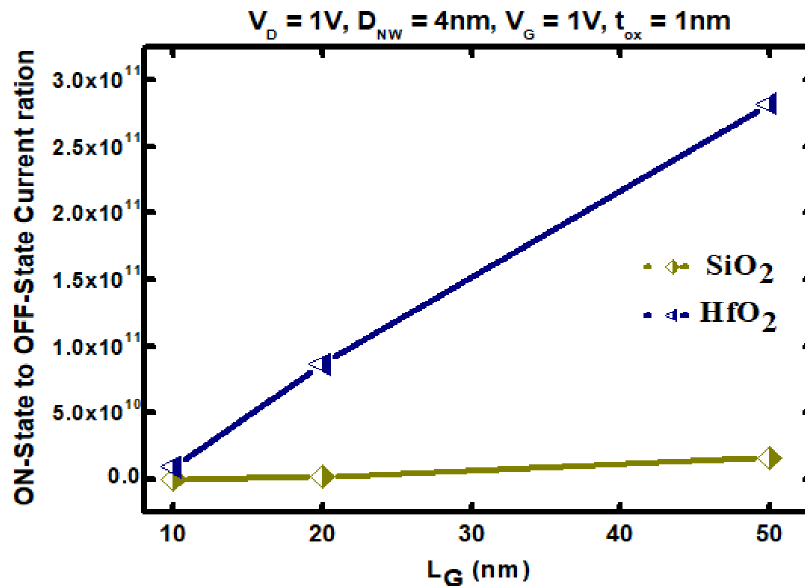

Figure 5 I_{ON}/I_{OFF} ratio of SiO_2 and HfO_2 FETs

Similarly, the performance continuous to increased when the gate length was increased to 50nm to 2.82 x 10^{11}A and 1.61 x 10^{10}A for HfO_2 device and SiO_2 device respectively.

6. CONCLUSION

Significant improvement of SCEs such as DIBL and subthreshold swing was observed in the NJT designed with HfO_2 gate oxide than device with SiO_2 gate oxide. The leakage and I_{ON} current in HfO_2 device were significantly improved due to the high dielectric constant and high gate capacitance. High doping concentration and small D_{NW} triggered the On-state current to increased due to full depletion of the heavily doped channel. Therefore, faster switching speed of the HfO_2 device was observed more than SiO_2 device as a result of highly improved On-state to Off-state current ration in the device.

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