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Design of MOSFET Based Boost Converter with PID and Genetic Algorithm Optimizer for Resistive Load

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ABSTRACT

The focus of this research is the development of a DC-DC boost converter employing a polymer-based MOSFET to ensure consistent output despite variations in Resistive (R)-load. An appropriate controller for the developed converter is designed through the application of diverse optimization techniques, aiming for straightforward implementation, improved convergence quality, and enhanced computational efficiency. The optimization of Proportional-Integral-Derivative (PID) controller parameters using various algorithms is performed to enhance the converter's dynamic response in the presence of R-load. To tune the PID controller, Genetic Algorithm optimization parameters are utilized, which enhance the efficiency while including R-load. The effectiveness is measured in overshoot, rise time, settling time and peak time. The analysis also encompassed time integral domain specifications, including Integral Square Error (ISE), Integral Absolute Error (IAE), and Integral Time Absolute Value Error (ITAE). The research modeling of this technique is done in MATLAB/SIMULINK 2018 platform by considering various performance metrices.

Keywords: Boost Converter, Genetic Algorithm, PID Controller, Resistive Load, MOSFET.

I. INTRODUCTION

Power electronics is a field that primarily focuses on converters employed at power levels rather than signal levels. Within a power electronic system, there exists one or multiple power electronic converters, which consist of power semiconductor devices that are under the control of integrated circuits, as detailed in [1]. Leveraging the switching capabilities of these power semiconductor devices, a power electronic converter is capable of converting input power from one form to the output power of another form, as elaborated in [2]. Power Electronics is also ushering in a new type of industrial revolution with its versatility in applications, such as conservation of energy, energy storage for bulk utility, renewable energy system, and industrial automation. In case of power conversion, a DC-DC converter acts an important role with the widespread applications of laptops, Light Emitting Diode (LED) drivers, cellular phones, electric vehicles, hydro power plants, maximizing the harvest of energy for photovoltaic systems and wind turbines, and so on in [3]. This application needs the converter to achieve increased efficiency, and Power Factor (PF) with the increase in availability [4]. A DC-DC converter either increases or decreases the input voltage, based on the need of the connected load, with the adjustment of the duty cycle applied to the switching device, based on Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) [5]. The schematic of a typical boost converter is depicted in Fig. 1.

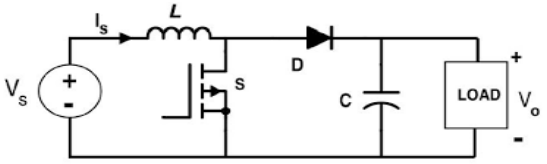

Fig. 1: Schematic of Boost Converter.

The converter depicted in Fig. 2 requires only four external components, such as diode, electronic switch, inductor, and an output capacitor. The converter can thus be operated in the two different modes based on its capacity to store energy and its relative duration of the switching period by [6]. In this context, the capacitor on the resultant side serves the purpose of minimizing voltage ripple, while an inductor on the input side is responsible for producing a ripple-free current that corresponds to the voltage [7]. The analysis of the boost converter is typically conducted under Continuous Conduction Mode (CCM).

During the ON state of the switch, the diode becomes reversed-biased, isolating the output stage and allowing the inductor to receive energy from the input. Conversely, when the switch is in the OFF state, energy is drawn from both the input side and the inductor to power the output. To maintain a consistent output voltage, a large output capacitance is employed. The power converters' output must adhere to a specific tolerance range to achieve the desired outcome by adjusting the set voltage. This achieved output is compared with a reference value, generating an error value utilized to regulate the converter's switch duty cycle through a control mechanism, as described in reference [8].

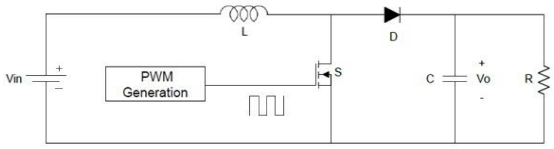

Fig. 2: DC-DC Boost Converter.

The term fitness is termed as the minimal value of error that is estimated as the change among the acquired value of the boost converter and the reference value. The error for fitness is estimated in Equation 1 for R load as,

$$V_{error} = V_{ref} - V_{out} \qquad (1)$$

The value of V_{out} represents the output from the converter and V_{ref} is the reference voltage. The fitness or the objective functions taken are rise time, settling time, ISE, IAE, and ITAE. The optimization is done using four optimization algorithm and is explained in below sections [9].

II. METHODOLOGY

The optimization process for the PID controller involves the utilization of four distinct optimization algorithms, and these procedures will be elaborated upon in the upcoming sections. The primary objective of this optimization is to fine-tune the PID controller's constraints to achieve optimum output within the considered system [10]. Each optimization algorithm brings its unique approach to parameter adjustment, which will be discussed comprehensively in the following sections. By employing multiple optimization techniques, a comprehensive exploration of the parameter space is ensured, enhancing the likelihood of identifying the most effective parameter values for the PID controller [11].

The Queen-Beee Genetic Algorithm (QBGA)-PID optimization is an iterative process that is performed till obtaining an optimum solution. By applying QBGA, the PID parameters are optimized. Algorithm parameters and the optimization problem are initialized. The optimization is performed to get optimum values for k_p, k_i and k_d. In this step, the optimization problem minimizes rise time, settling time, ISE, IAE, and ITAE, and the decision variables (n) are defined. In addition, the population size (R), the recombination probability (P_r), and the epoch count (I_{max})are also defined [12]. The objective function is represented in Equation (2) as.

$$F(x) = (1+t_s)(1+E_{ISE})(1+E_{IAE})(1+E_{ITAE}) \qquad (2)$$

where, $F(x)$ is the objective, in terms of rise time t_r, settling time t_s, ISE, IAE, and ITAE, and D is the count of decision variables. The parameters of QBGA algorithm are also specified in this step.

During the generation of bees**,** the number of bees that are involved in the solution space be represented as B_1, B_2,……B_i,……, B_n where n is bees' population. Among the bees that are generated in random, the best queen bee B_q

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minimize $F(x)$. PID is simulated digitally with all the bees, and $F(x)$ is evaluated for each bee. Equation (3) provides the queen bee from the n number of bees, denoted as B_q.

$$B_q = Max\left(\frac{1}{1+F\left(x_i\right)}\right) \qquad (3)$$

Thus, the best queen bee is obtained from Equation (3) and is separated from others. Not all drones possess the ability to swiftly reach a queen bee, which prompts the incorporation of a recombination probability associated with all drones [13]. To achieve this, a recombination probability denoted as "p" is introduced, constrained within the range of 0 to 1. Each drone's probability is represented as "p_d". When the condition "$p_d \leq p$" is met, the queen bee engages in recombination with the drone, leading to the creation of two virgin queen bees. This process mirrors the concept of crossover in the standard Genetic Algorithm (GA). While the QBGA framework elaborates the crossover for a single parameter for clarity, employing multipoint crossover is recommended for enhanced efficacy [14]. Recombination results in two offspring, of which only the fittest is retained, akin to the virgin queen bee discarding one offspring. A schematic representation of the QBGA optimization process for the PID controller is depicted in Fig. 3.

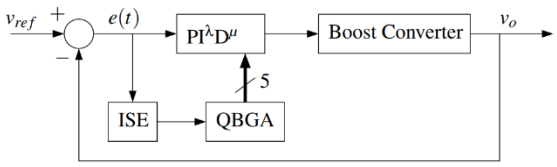

Fig. 3: Tuning and Optimization of PID Parameters using QBGA.

In a bee hive, there occur a fight between all the virgin queens, and only the fittest virgin bee survives. The entire population, comprising both virgin and mother queen bees, undergoes evaluation using Equation (3). This evaluation process assists in identifying a new queen bee. Subsequently, all the bees except for the selected queen bee are removed from the hive. The program concludes when the termination criterion is met, and the newly generated queen bee is considered the optimal solution.

Table 1: Parameter setting of QBGA –PID

Parameters	Values
Decision variables, n	10
Population size, R	10
Probability of Mutation	0.2
Probability of Cross over	0.8
Recombination probability P_r	0.8
No of iteration, I_{max}	500

III. RESULTS AND DISCUSSIONS

The entire framework implementation is executed in MATLAB/SIMULINK environment. The best control parameters for QBGA algorithm were selected, and the *.m files* were performed to partition the data of fitness and the gain values. The algorithms were executed with 10 simulation-runs. Each simulation-run has 500 numbers of iterations. The count of simulation runs acts as stopping criteria in QBGA algorithm. From the overall simulation-runs, the runtime that returned the least fitness and best optimal solution was selected. The solution is enhanced in all successive iterations and the process is continued until finding the optimal solution. The simulation is done with R-

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load and RLE-load for QBGA tuned PID controller. Thus, QBGA tuned PID were used to find the better parameters of fitness k_p, k_i and k_d. Gain Parameters obtained for various PID controllers are provided in Table 2.

Table 2: Gain Parameters of various PID Controllers

Methodology	k_p	k_i	k_d
QBGA Tuned PID	0.8101	0.6863	0.0220
SFLA Tuned PID	1.4392	0.6032	0.01223
CSA Tuned PID	1.0734	0.6336	0.0234
FFA Tuned PID	0.9001	0.8844	0.0781

The comparative analysis of performance indices with R-Load is depicted in Table 3. The value of ISE using QBGA tuned PID controller, SFLA tuned PID controller, CSA, and FFA are 0.3048, 0.0905, 0.0807, and 0.0706, respectively. Similarly, the value of IAE using QBGA tuned PID controller, SFLA tuned PID controller, CSA, and FFA are 0.6118, 0.1717, 0.1265, and 0.1123, respectively. The value of ITAE using QBGA tuned PID controller, SFLA tuned PID controller, CSA, and FFA are 0.1657, 0.0802, 0.0638, and 0.0456, respectively. Thus, from the Table 3 it is evident that FFA tuned PID controller has reduced ISE, IAE and ITAE as compared to other optimization algorithms.

Table 3: Comparative Analysis of Performance Indices (R-Load)

Type of Error	QBGA Tuned PID	SFLA Tuned PID	CSA Tuned PID	FFA Tuned PID
ISE	0.3048	0.0905	0.0807	0.0706
IAE	0.6118	0.1717	0.1265	0.1123
ITAE	0.1657	0.0802	0.0638	0.0456

Fig. 4 depicts the comparative response curve with respect to QBGA, SFLA, CSA and FFA based PID controller ISE with R-load. From the response curve it is evident that FFA converges faster when compared to QBGA, SFLA and CSA.

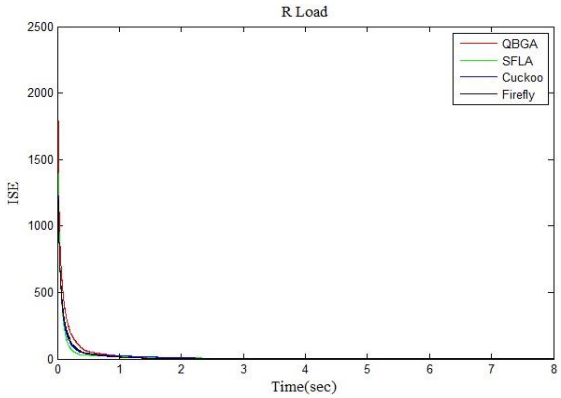

Fig. 4: Comparative Response Curve with Respect to QBGA, SFLA, CSA and FFA Based PID Controller ISE with R-Load.

Fig. 5 depicts the comparative response curve with respect to QBGA, SFLA, CSA and FFA based PID controller ITAE with R-load. From the response curve it is evident that FFA converges faster when compared to QBGA, SFLA and CSA.

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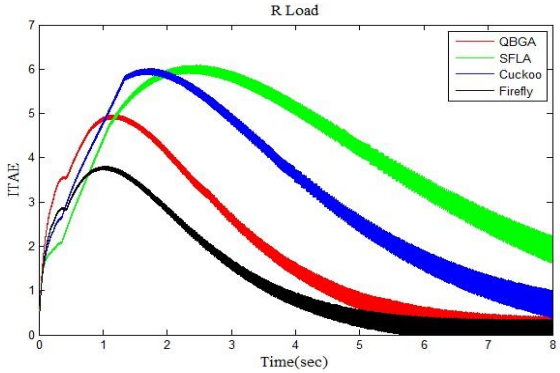

Fig. 5: Comparative Response Curve with Respect to QBGA, SFLA, CSA and FFA Based PID Controller ITAE with R-Load.

Fig. 6 depict the comparative response curve with respect to QBGA, SFLA, CSA and FFA based PID controller IAE with R-load. From the response curve it is evident that FFA converges earlier when compared to QBGA, SFLA and CSA.

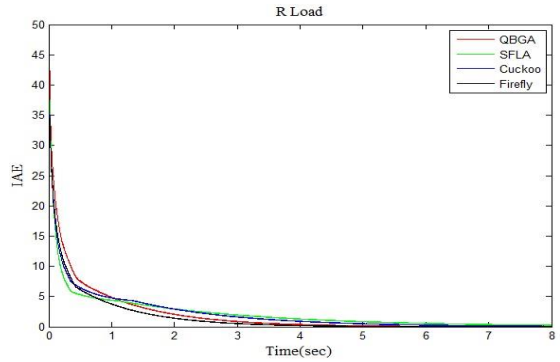

Fig. 6: Comparative Response Curve with Respect to QBGA, SFLA, CSA and FFA Based PID Controller IAE with R-Load.

Fig. 7 efficiency of QBGA, SFLA, CSA and FFA based PID controller with R-load. The efficiency noted in FFA based PID controller with resistive load is 84% which outperforms QBGA, SFLA and CSA.

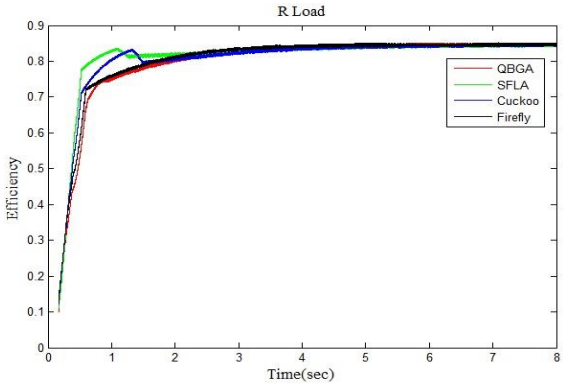

Fig. 7: Efficiency of QBGA, SFLA, CSA and FFA based PID Controller with R-Load.

Table 4: Comparative Analysis for Time Domain Specifications (R-Load)

Parameters	QBGA	SFLA	CSA	FFA
Rise Time (sec)	0.5150	0.4253	0.4170	0.3170
Settling Time (sec)	2.2602	1.9762	1.7062	1.2442
Settling (Max) (V)	48.01	47.92	47.989	48.0192
Peak Over Shoot	0.048	0.054	0.0460	0
Peak Value (V)	48.01	47.92	47.989	48.0192

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The comparative analysis of the time domain specification for QGBA, SFLA, CSA, and FFA with R-load is tabulated in Table 4. The rise time obtained using the algorithms, such as QGBA, SFLA, CSA, and FFA is 0.5150sec, 0.4253sec, 0.417sec, and 0.317sec, respectively. Similarly, the settling time obtained using the algorithms, such as QGBA, SFLA, CSA, and FFA is 2.2602sec, 1.9762sec, 1.7062sec, and 1.2442sec, respectively. Results indicates that the utilization of the QBGA gives greater improvement in time domain.

IV. CONCLUSION

This paper discusses the need for the proposed FFA algorithm in tuning the PID parameters in such a way to maintain constant output at the output of the boost converter. By dynamically adjusting the duty cycle of the boost converter based on the optimally tuned PID controller, the efficacy of this novel approach is systematically assessed by comparing it to conventional methods. Evaluation metrics encompass critical factors as well as integral performance indices, including ISE, IAE, and ITAE. The obtained outcomes distinctly demonstrate the effectiveness of the proposed QBGA in fine-tuning the PID controller's parameters. Moreover, an in-depth examination of the system's dynamic response employing the proposed QBGA reveals its enhanced effectiveness in comparison to alternative optimization algorithms. Therefore, it is evident that the proposed QBGA showcases superior performance, significantly aligning with the predetermined objectives of the study.

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